

Vol. 65 • No. 10

October 2022



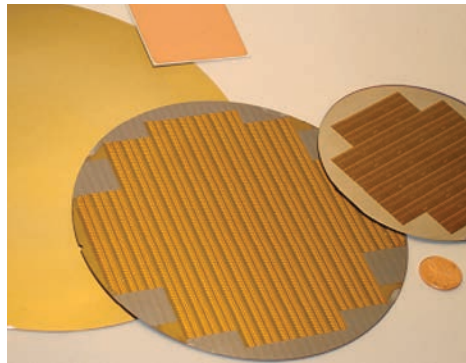
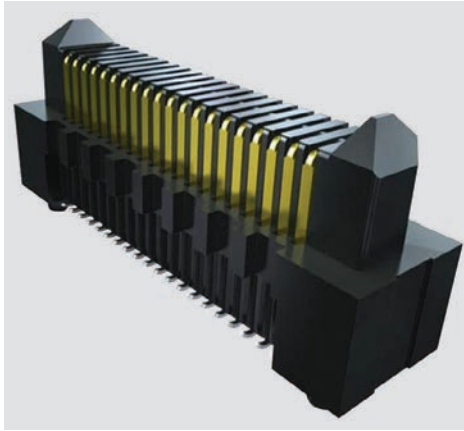
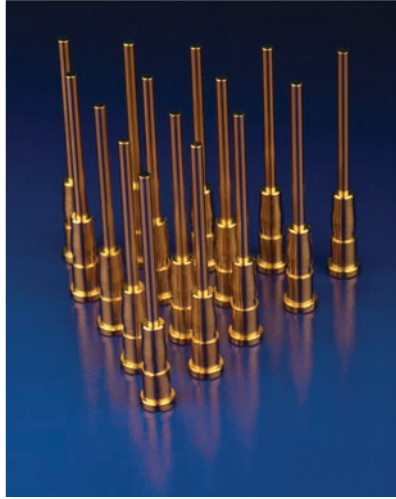
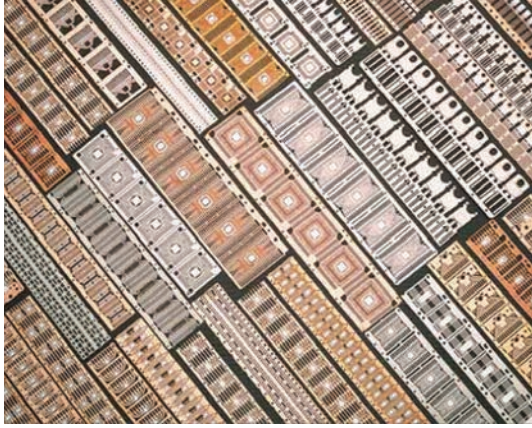
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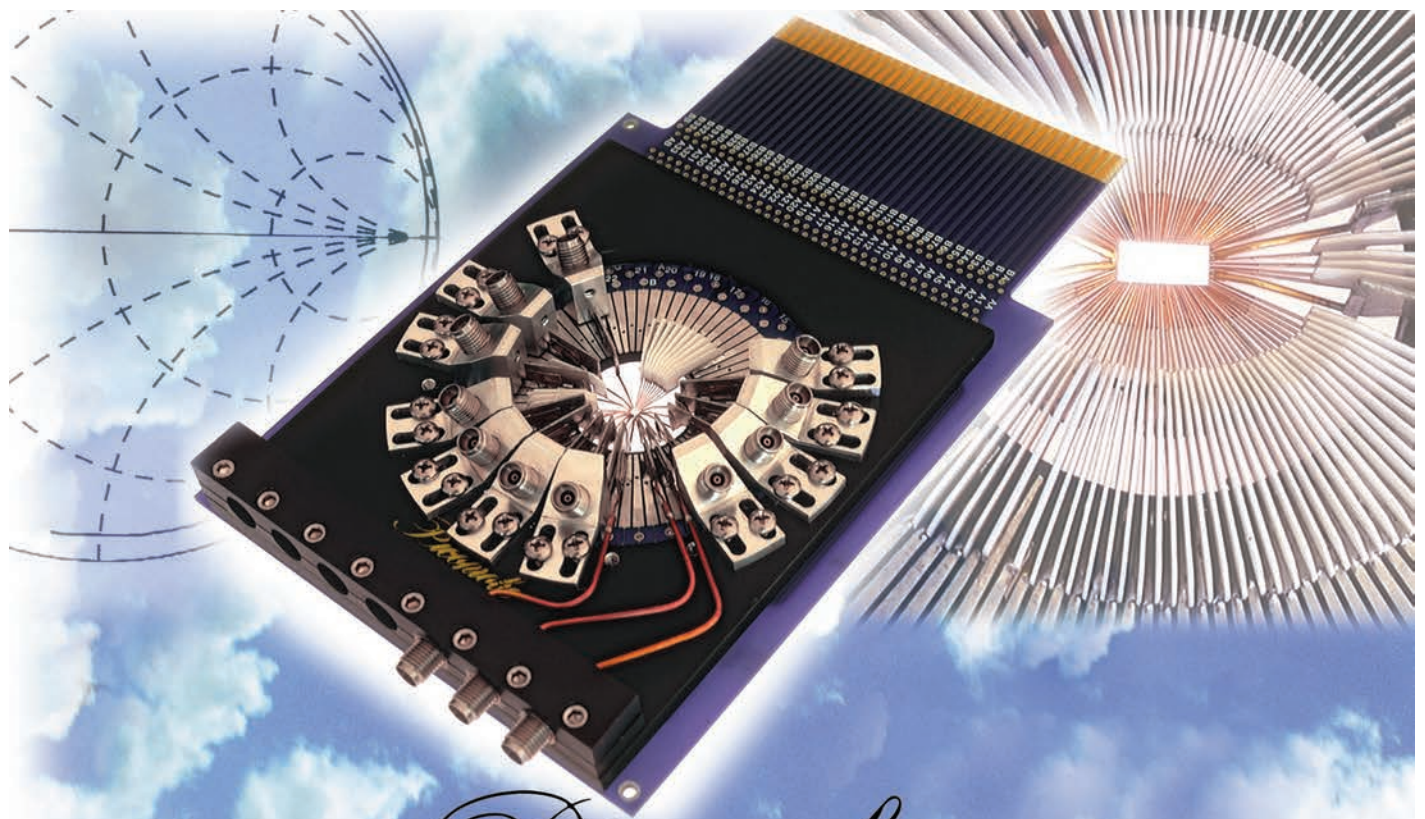
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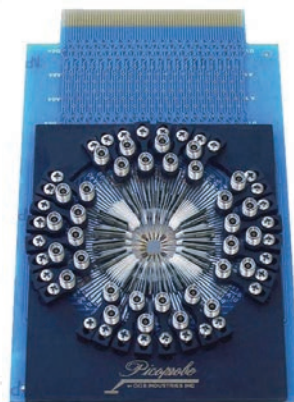
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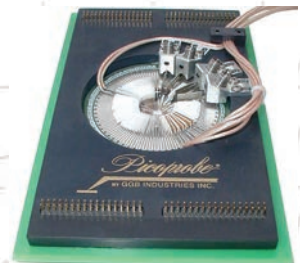


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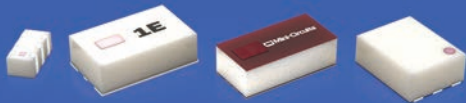
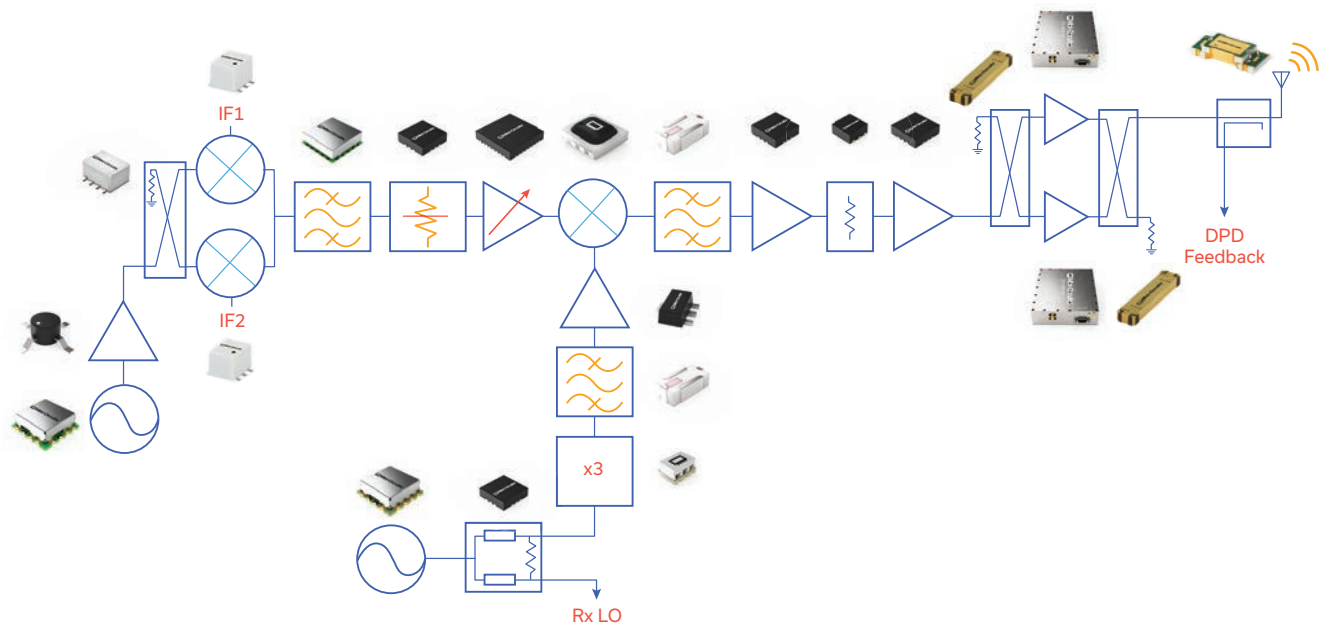
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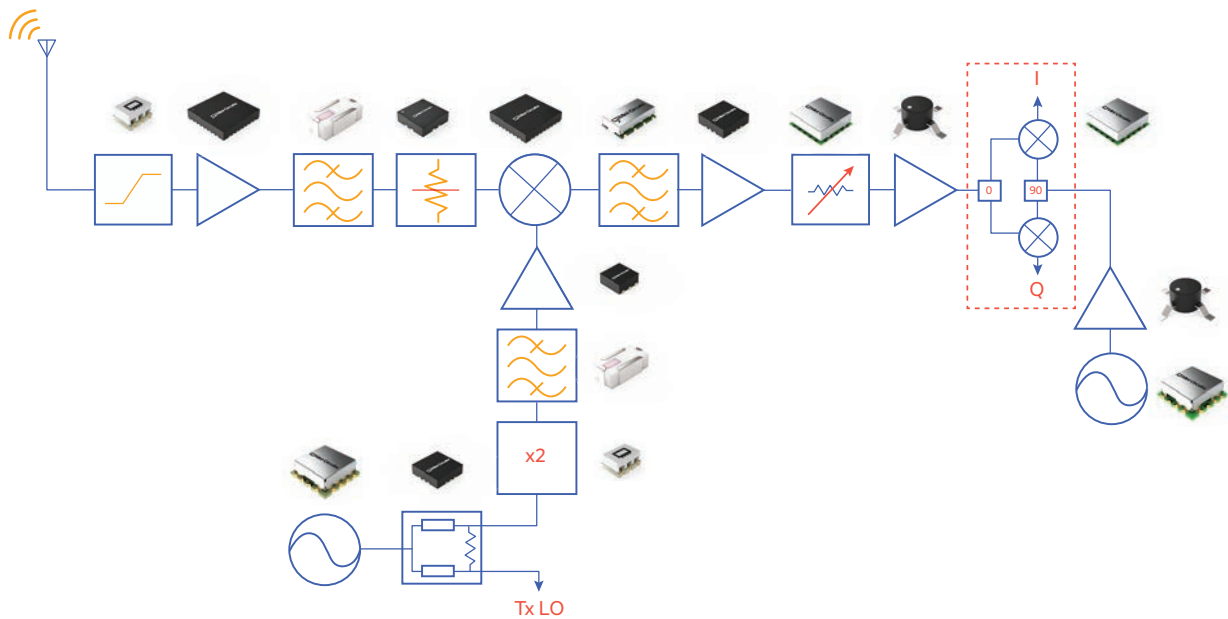
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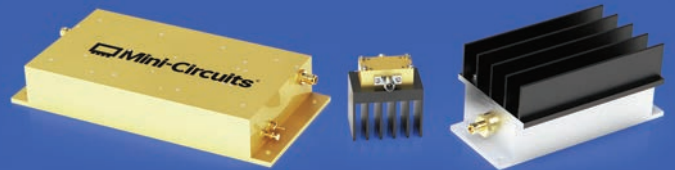


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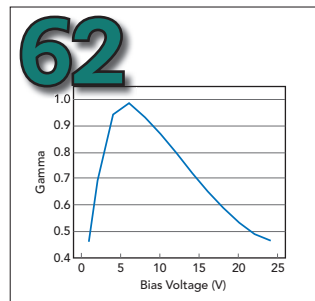
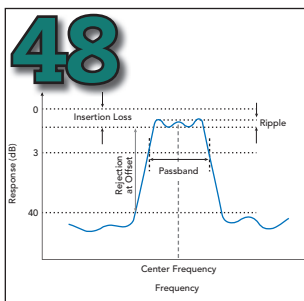
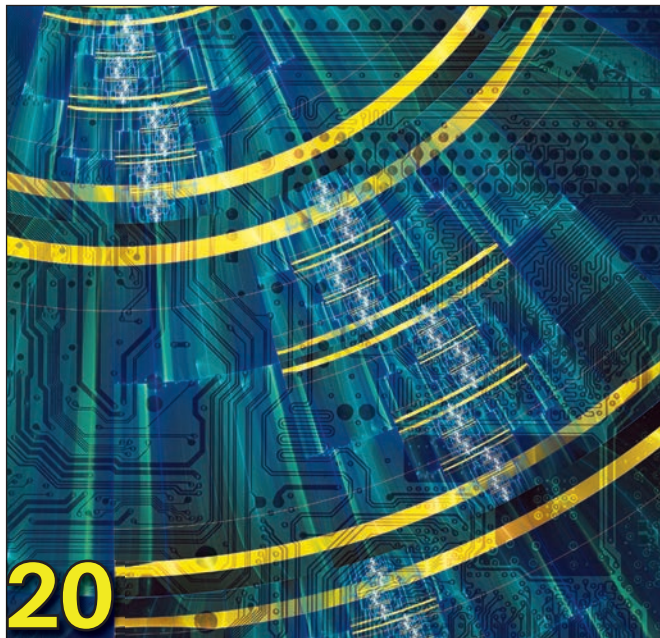
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Dimov Stojce Ilcev

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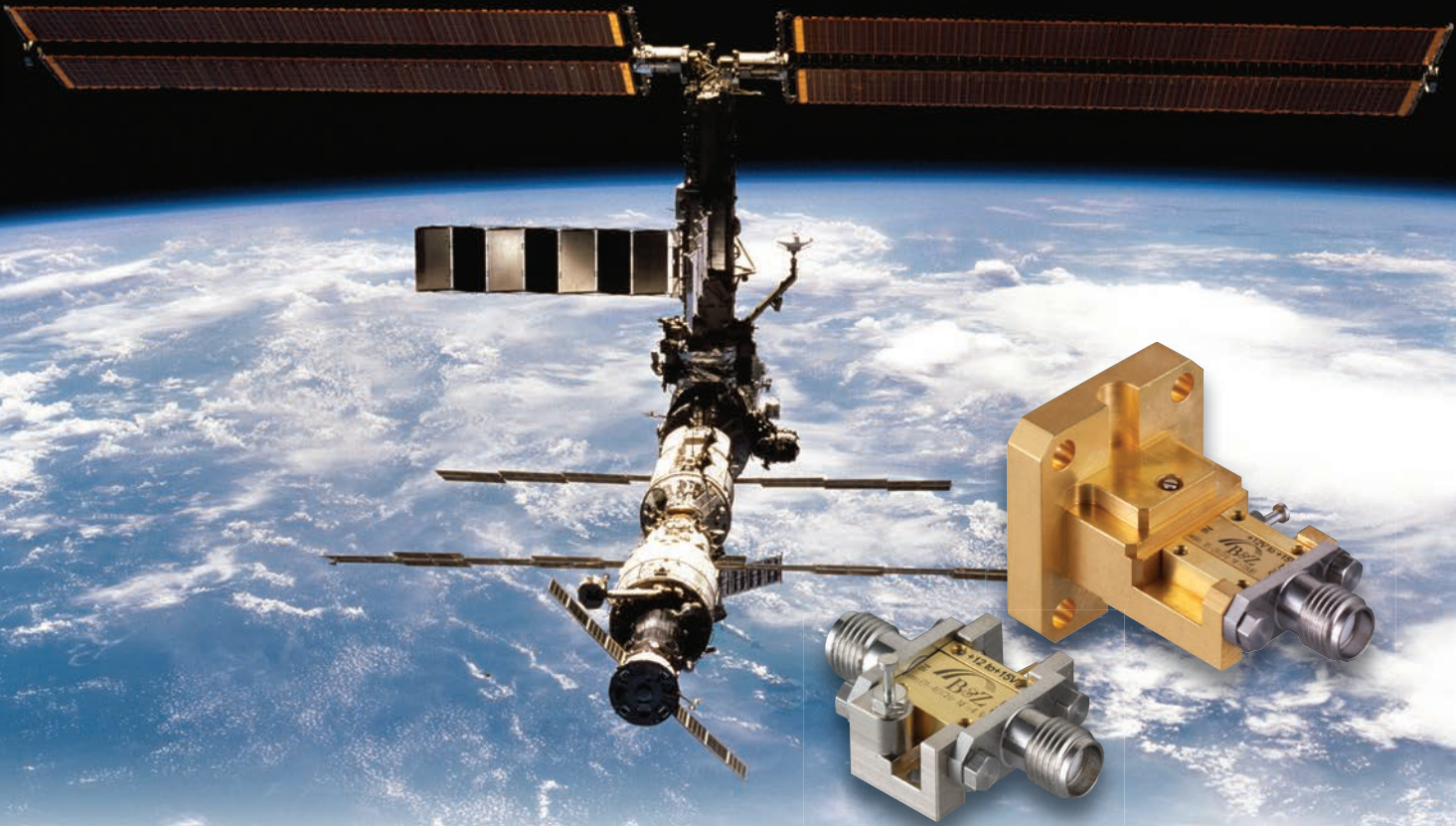
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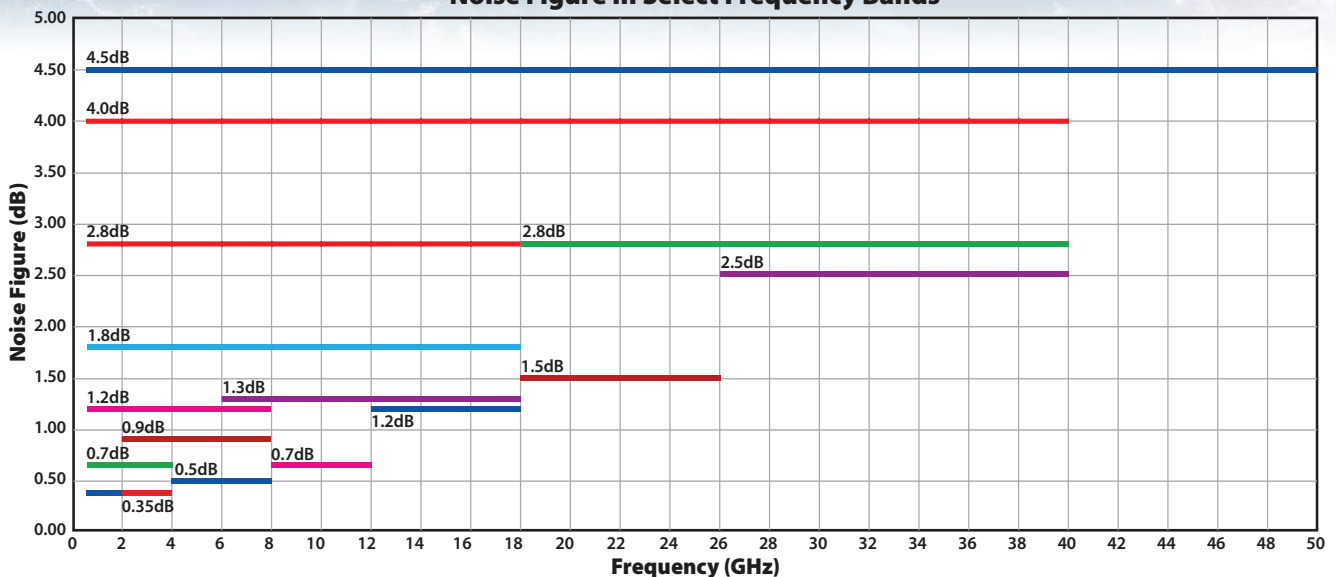
Peter Matthews, Knowles Precision Devices

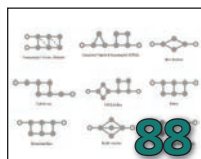


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Product Feature

88 Topology Library Streamlines Complex Filter Design, Reducing Development Risk

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ERRATUM

In the article "Pasta, Pizza and "Parlando di Microonde," published in the August 2022 issue of Microwave Journal, Rome is noted as the founding location for Microwave Filters & TVC. The company was actually founded in Milan.

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Microwave Journal (USPS 396-250) (ISSN 0192-6225) is published monthly by Horizon House Publications Inc., 685 Canton St., Norwood, MA 02062. Periodicals postage paid at Norwood, MA 02062 and additional mailing offices.

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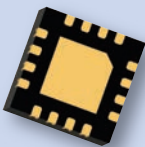
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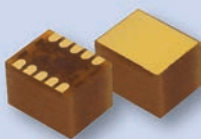
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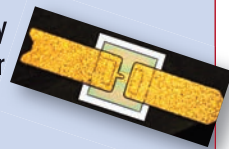
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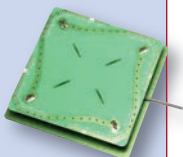
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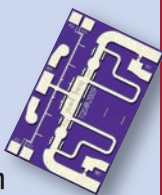
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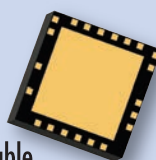
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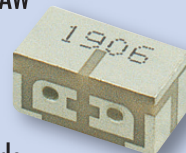
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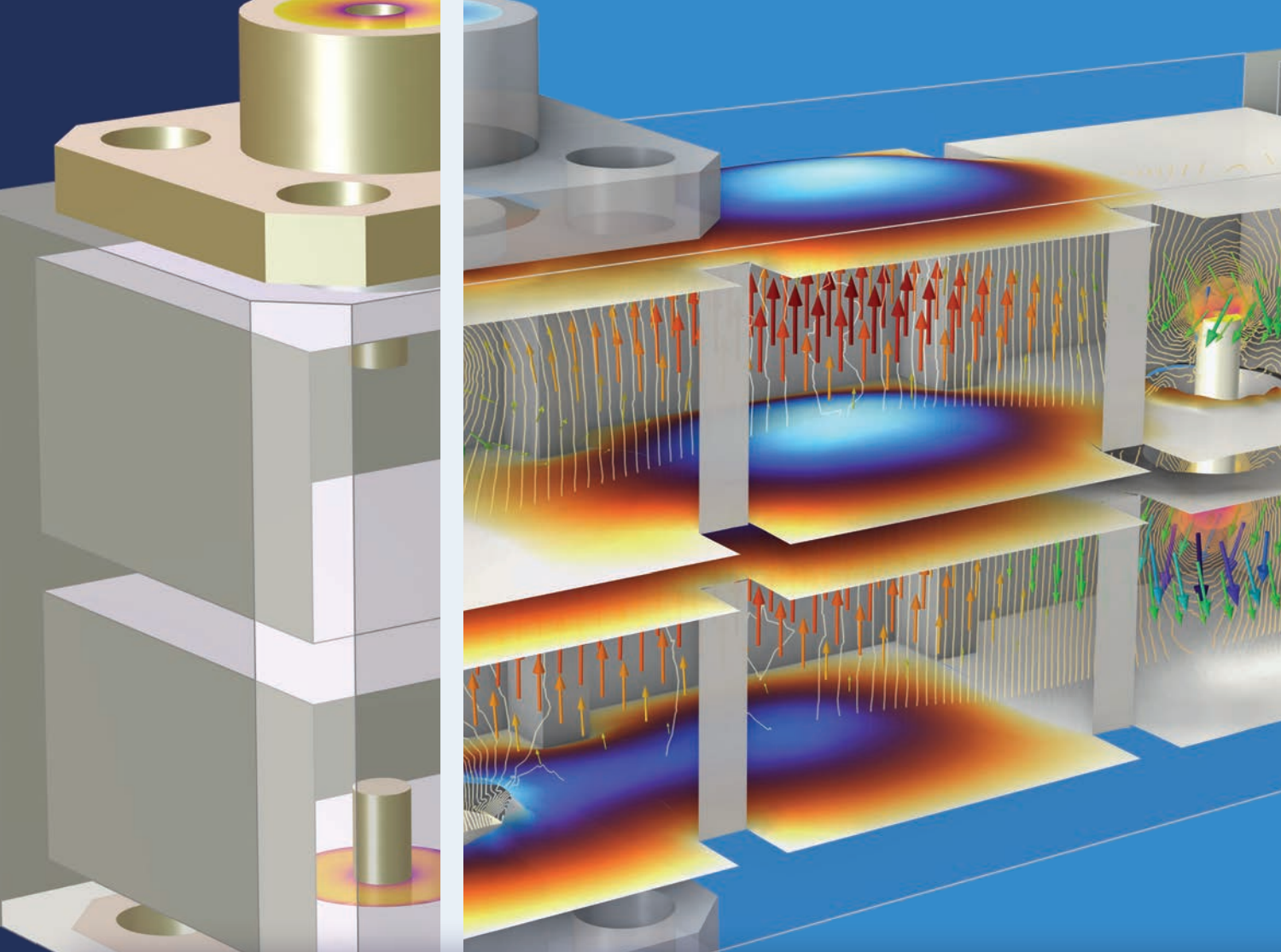


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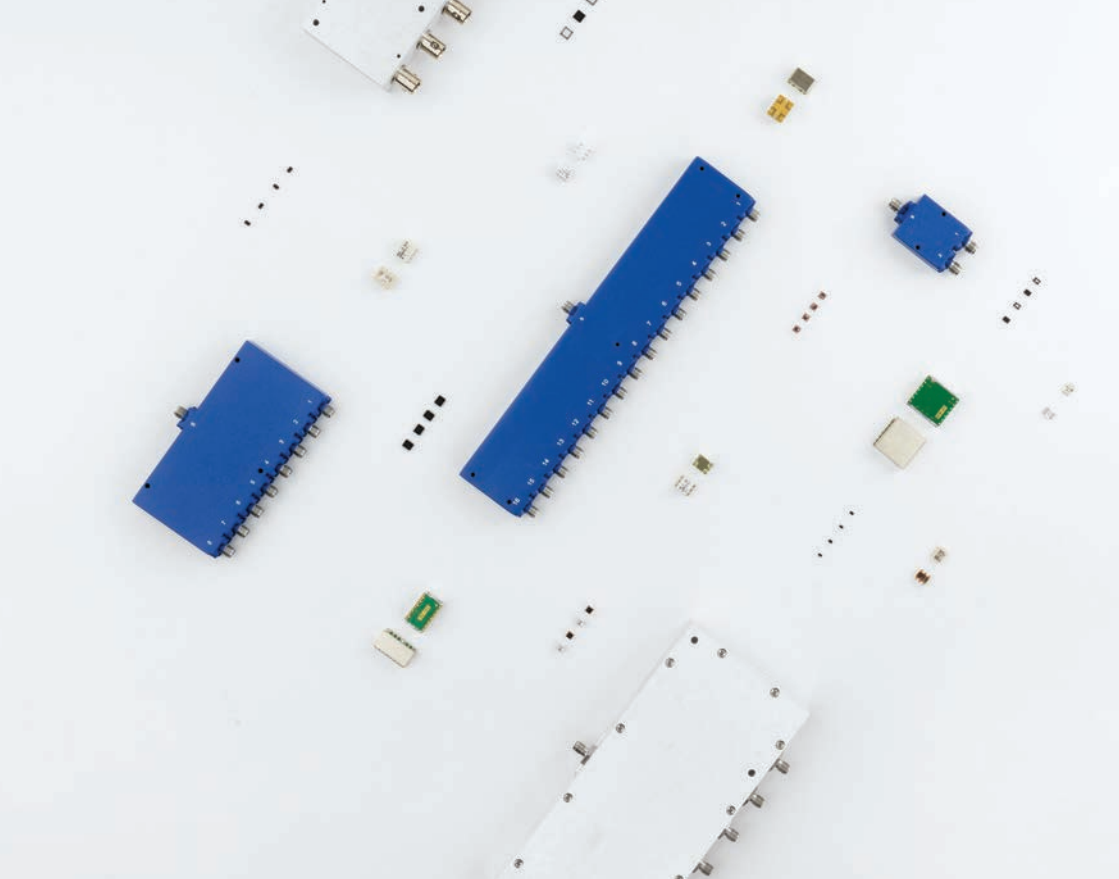


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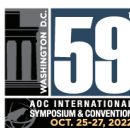
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PCB Design Considerations for mmWave

Niels Kirkeby, Chong Mei and Tom Buck
TTM Technologies, Santa Ana, Calif.

In the last decade, there has been an evolution to mmWave applications (i.e., 24 to 100 GHz) for commercial, industrial, IoT, wireless connectivity and an array of automotive radars. This rapid growth of mmWave applications has created a demand for multilayer printed circuit boards (PCBs) with mmWave circuits. The transition to mmWave comes with many challenges for the printed circuit industry—primarily conductor geometries and materials, since the shorter wavelengths reduce feature sizes and magnify the relative tolerances inherent in the PCB manufacturing processes. This article aims to help engineers design mmWave PCBs with good manufacturability and consistent electrical performance and to avoid some common design errors. Considering all key areas of PCB design, we introduce critical dielectric and conductor material properties, along with manufacturing process challenges.

Controlling production costs can

be a complex engineering challenge. Cost must be incorporated into the electrical design from the very start, since this is where materials, substrate architecture and PCB technologies are defined. Like all good engineering, the goal is to design a product meeting all performance requirements with high yield, accounting for all material and manufacturing tolerances—resulting in a trade-off between cost and performance.

Finally, conducting signals to different layers is a difficult problem at mmWave frequencies. Leveraging material properties and the manufacturing challenges, we show an example of the formation of various via structures for mmWave PCB applications. We introduce a surface mountable crossover component simplifying via formation that has several additional advantages. It facilitates rapidly changing architectures and conducting signals to different layers, addressing the impact on electrical performance.

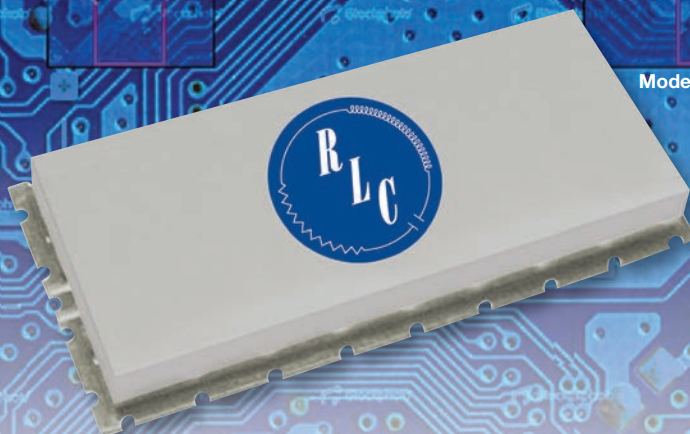
PCB MANUFACTURING CHALLENGES

mmWave wavelengths are the same order of magnitude as PCB geometries. Cost is another factor adding to design complexity, since many new mmWave products are for consumer applications where substrate production volumes range from tens of thousands to millions of units.

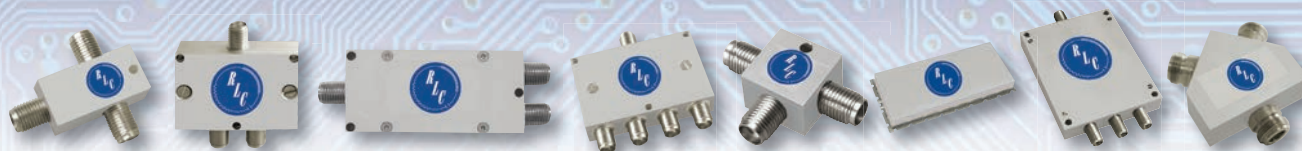
In its simplest form, printed circuits are fabricated using a photo imaging and chemical etching process. This is accomplished by taking a copper clad laminate or a multilayer laminate and drilling circuit holes. After drilling, the panel is electroplated, building up copper in the drilled holes and on the surface—about 2 mils thick when starting with half an ounce of copper foil. Next, a photo resist is applied to the surface, imaged through a photo mask using ultraviolet light and developed to expose the unwanted copper. The exposed copper is chemically etched, leaving a

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finished circuit. This is defined as a "panel plate" process.

Etching down to the dielectric also etches laterally into the side of the conductor, making the process generally unsuitable for RF/microwave applications: Both electroplated copper and the base foil must be etched to form the conductor, resulting in poor geometries and less than desired conductor tolerances.

To overcome the problems with panel plating, most circuits are fabricated using a "pattern plate process." Instead of electroplating the entire panel surface, photo resist is applied over the base copper foil. Then, either a photo mask or laser direct imaging is used to transfer the circuit image to the resist coated panel. After imaging and development, the areas exposed on the base copper foil will be electroplated, forming a circuit pattern with copper also in the drilled holes. To protect the circuit image and hole barrels from the final etch, tin is plated on top of the circuit image. Next, the photo resist is stripped, and the background copper foil is etched, followed by a tin strip, yielding a finished circuit. The pattern plate process provides better geometries and tighter tolerances than panel plating because only the base foil needs to be chemically etched, minimizing the lateral etch that alters the conductor side walls (see **Figure 1**).

mmWave designs operating from 60 to 100 GHz require improved conductor tolerances and corner radius specifications on antenna patches and inset feed lines. Several technologies have been introduced to achieve tighter etching tolerances. The first involves the reduction of the base copper foil thickness on critical layers by chemical milling. The base copper foil is reduced to less than half an ounce, which reduces etching time and improves conductor geometries, minimizing etching into the conductor sidewalls and etch compensation. A second approach developed for mmWave applications, which enables tighter tolerances; smaller, undercut and better resolution; is a modified etch additive process (MEAP). Much like the foil reduction process, MEAP takes advantage of thinner base copper; however, it uses advanced etching technology to produce an extremely uniform copper geometry after etching (see

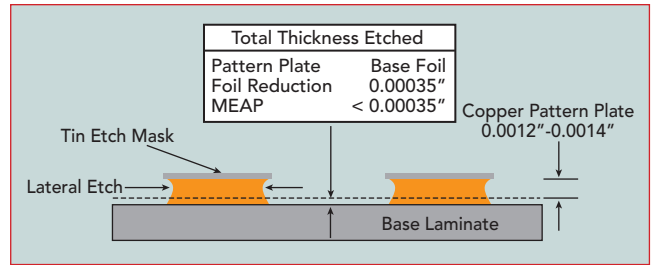


Fig. 1 Lateral etch thickness for the foil reduction and advanced foil reduction processes.

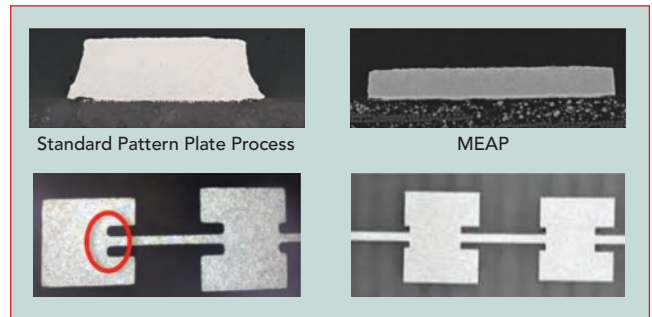


Fig. 2 Standard pattern plate process and MEAP.

Figure 2).

Another factor often overlooked is the additional copper thickness, due to more complex via structures, impacting both conductor geometries and tolerances. Most advanced PCB structures incorporate more than just through holes. There are also blind vias, buried vias, micro-vias and "via in pad plated over" (VIPPO), which complicate the plating process. To create reliable via holes, the copper must be plated from the circuit pattern surface down the hole barrel and back

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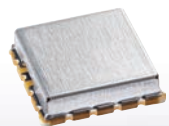
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to the termination surface. Known as "wrap plating," the copper plating is continuous, with no grain boundary that can fail in thermal cycling or assembly. Wrap plating occurs by default with through holes, since all three surfaces are plated simultaneously. This is not the case with blind via and VIPPO. Per the IPC-6012 specification, a panel plate is required to meet a minimum thickness of 0.0002 in. per wrap plating cycle (see **Figure 3**).

Designs at mmWave almost always have a requirement for VIPPO and or blind vias to one or more depths. The implication for simulation models is that the base foil now has an additional copper plating thickness of 0.0002 in. minimum per wrap cycle. The additional copper thickness affects the conductor resolution as well as the tolerance of the electrical design. For example, adding VIPPO adds one wrap plating cycle; two blind via depths adds two wrap plating cycles; etc. This must be addressed early in the design process.

A third process is introduced to maintain accurate dimensional tolerances and to overcome copper thickness variations. This process is a hybrid between a pattern plate

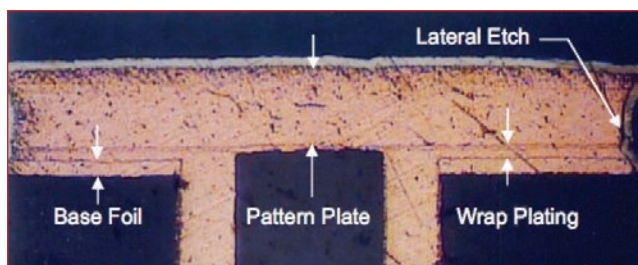


Fig. 3 VIPPO vs. wrap plating.

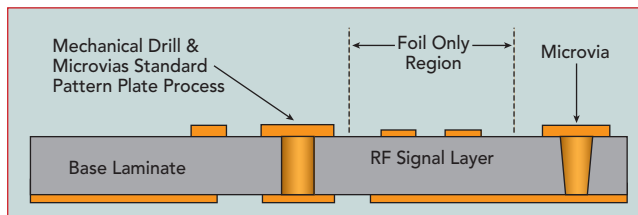


Fig. 4 C²eT process.

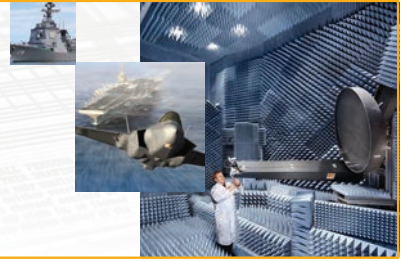
and a simple foil print and etch. The concept is straightforward for circuit images such as patch antennas and filter transformers: they are photo imaged on the base copper foil, usually half an ounce or less, then etched. The etched features are not plated, having the benefits of a foil-only etch and a thickness tolerance based only on the base copper foil. Non-critical and solder locations are plated with a standard pattern plate process (see **Figure 4**). While this process, known as C²eT, adds cost from the extra process steps, it offers better electrical performance.

Table 1 compares the features and capabilities of these PCB process technologies.

Simulation is the most important tool in the design process, defining the acceptable tolerances that determine what process technology is needed for conductor formation,

TABLE 1 PROCESS CAPABILITIES					
	Pattern Plate + VIPPO	Pattern Plate	Pattern Plate With Cu Reduction	C ² eT	MEAP
Line Width Tolerance	±25 µm	±20 µm	±18 µm	±18 µm	±15 µm
Line Width & Space CPK	> 1.33	> 1.33	> 1.33	> 1.33	> 1.33
Undercut (Cu Thickness)	≤ 35 µm (25 µm Minimum)	≤ 35 µm (25 µm Minimum)	≤ 16.5 µm (25 µm Minimum)	≤ 17.8 µm (18 ± 5 µm)	≤ 10 µm (35 ± 10 µm)
Corner Radius (Sharpness)	≤ 25 µm	≤ 25 µm	≤ 15 µm	≤ 15 µm	≤ 10 µm

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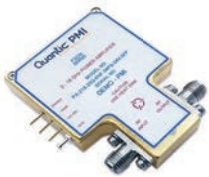


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dielectric materials and copper foil selection. Simulation is critical for cost reduction and failure analysis, since both are studied in a virtual environment that provides results faster than building prototypes.

Raw Material Tolerances and Variation

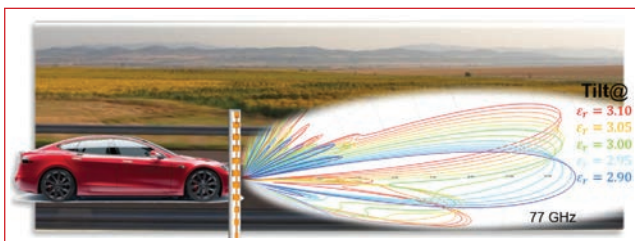
Regardless of the manufacturing process, manufacturing tolerances must be considered: both the raw materials, such as substrate and copper foil, and the PCB manufacturing process. Besides lot-to-lot variations and panel-to-panel variations, tolerances are often assumed to be global; however, they are also localized. Substrate effective dielectric constant (ϵ_{reff}) varies locally from non-homogeneous dielectric and the copper foil. The design itself affects the outcome. For example, the locations of vias affects the plating consistency by causing non-uniform currents, and variations in the copper percentage compounded through several layers may create localized peaks and valleys, causing irregular effective substrate heights after pressing. PCB manufacturing introduces localized differences from etchant/plating flow patterns that depend on direction.

One of the metrics that concern designers is the ϵ_{reff} of a design feature or object. For example, consider a PCB patch antenna used in an automotive medium to long-range radar at 77 GHz. The tilt of the elevation pattern will vary based on the ϵ_{reff} (see **Figure 5**). A 1 percent change in the dielectric constant of the patch antenna string is equivalent to a 0.74-degree tilt.

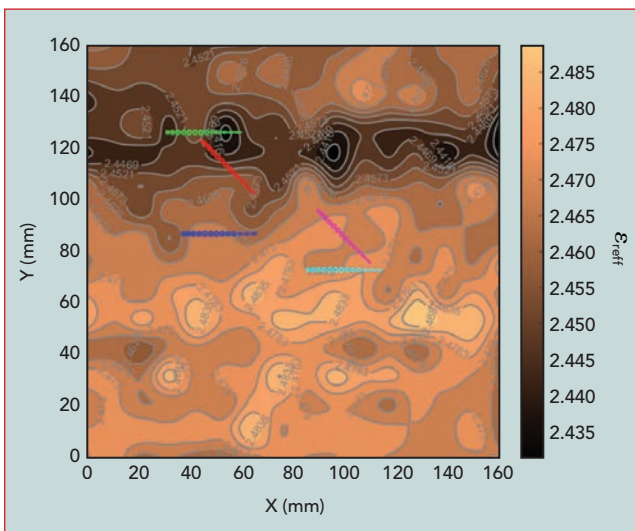
Any variation based on the designed board can

be optimized with one or more prototype builds. Substrate and PCB manufacturing tolerances are known and controlled within a range that can be included in simulations to enable centering the design. However, the controls may not correlate perfectly with what an RF object will experience. Substrate dielectric is measured and controlled by itself, copper foil is controlled by itself and both are spot sampled. PCB manufacturing is controlled by verifying the specific dimensions in discrete locations. But what is the combined variation of the key parameters within a panel?

To evaluate these effects, a 16×16 grid of ring resonators were measured on a typical RF substrate, developing a detailed map of the ϵ_{reff} (see **Figure 6**). The average is 2.47 with variation of ± 1.4 percent. An antenna array fabricated on the substrate could be located and oriented anywhere on the panel, as shown in the figure. While each patch in the antenna is small compared to the entire antenna, it could see the range of the effective di-



▲ **Fig. 5** Simulated tilt vs. dielectric constant for a 77 GHz antenna array.



▲ **Fig. 6** Effective dielectric constant from 16×16 measurements across 160×160 mm, with a 77 GHz antenna array overlaid in several locations and orientations.

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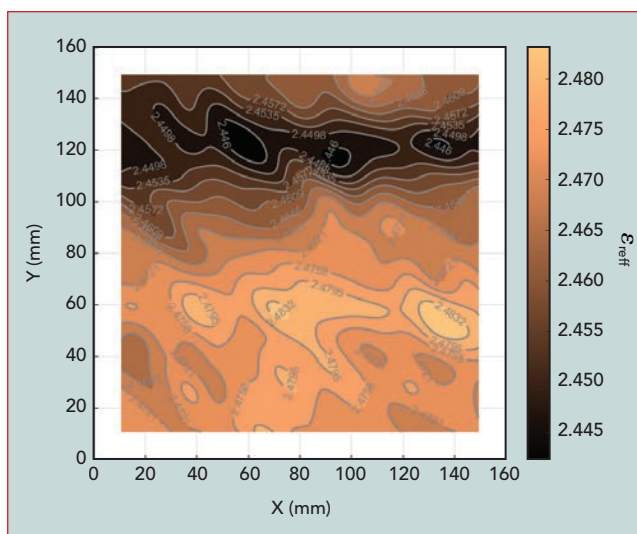
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electric constant variation depending on placement. It may be more useful to know the variation in ϵ_{reff} averaged over the entire antenna array. This can be derived by placing the antenna in all possible locations and orientations and calculating the average ϵ_{eff} underneath the array—ideally including significant fringing fields. In this calculation, with the antenna array overlaid at 45 degrees,

the average ϵ_{eff} is 2.47 with variation of ± 0.9 percent (see **Figure 7**).

Summarizing, a small feature such as an individual antenna patch at 77 GHz sees the full range of the ϵ_{reff} variation, here 2.47 ± 1.4 percent, where the whole antenna string array experiences an average of 2.47 ± 0.9 percent. As an entity, the antenna array experiences significantly less variation on average. Similarly, the system variation of ϵ_{reff} for all transmit (Tx) and receive (Rx) antennas combined would be further reduced. The localized variation is a product of all factors, such as localized variation in foil and substrate dielectric, PCB manufacturing processes and board design. Localized, lot-to-lot and panel-to-panel variations and tolerances depend on the specific material and process used, but tolerances will always be present.

Note that the dielectric constant derived from ring resonator measurements may not correspond exactly to the value experienced by an antenna or other circuit. Similarly, any measurement has some tolerance and repeatability. For this experiment, the measurement repeatability was characterized to ± 0.3 percent. The averages developed for the mmWave patch antenna discussed here may not fully characterize the variation in performance of another mmWave circuit; nonetheless, the example illustrates the concepts.



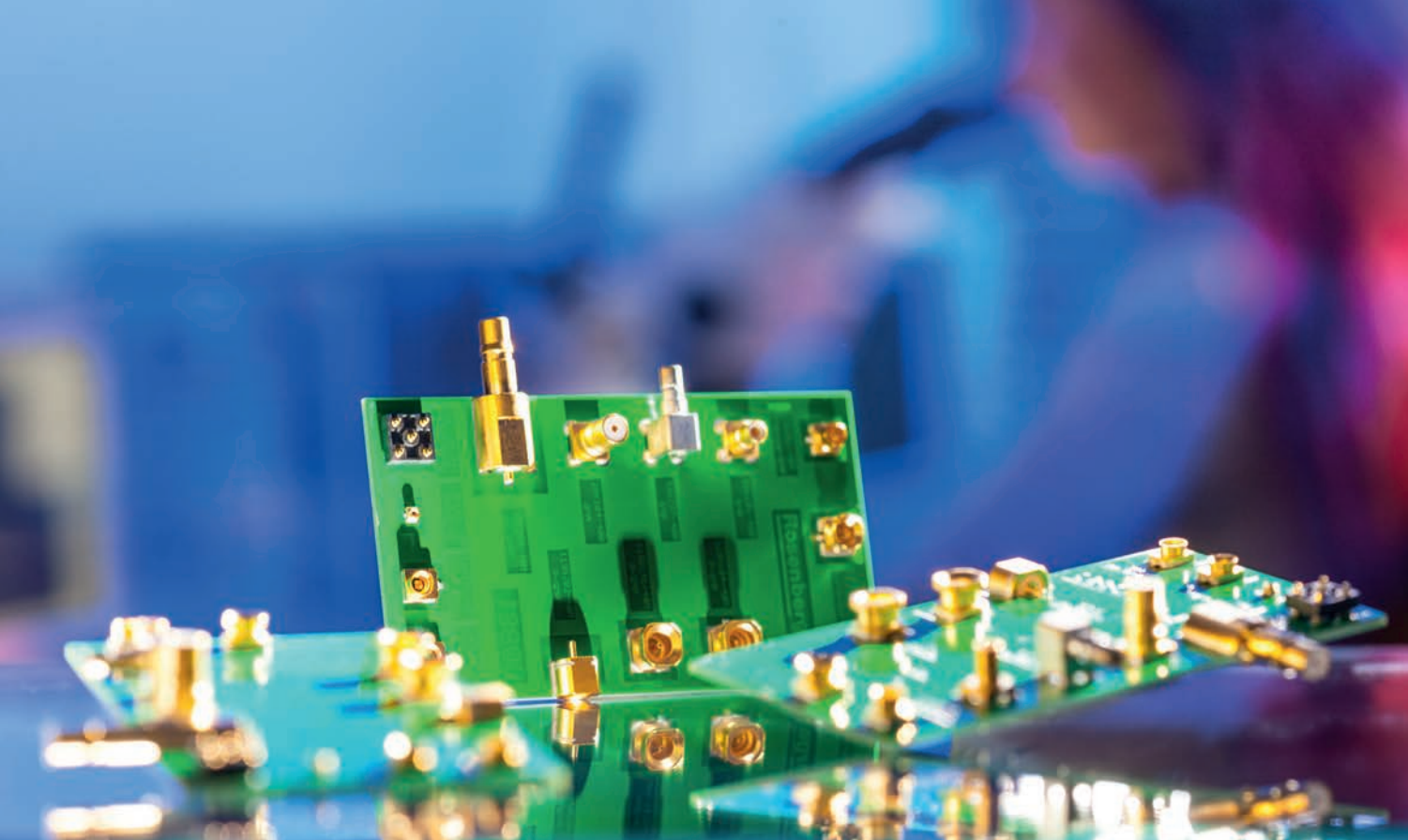
▲ **Fig. 7** Average effective dielectric constant for the 77 GHz antenna array when placed at 45 degrees anywhere within the measured area.

When designing an RF system, the manufacturing process must be selected to accommodate system needs, and the material and processing tolerances lot-to-lot, panel-to-panel and within the panel must be considered. Often, there are other system considerations which may impact both the manufacturing process and the resulting tolerances and must be considered. For example, the RFIC can be placed on the antenna side or the opposite side of the PCB.

COMPONENT SOLUTIONS

Conducting signals to different layers using vias is very common. The mismatch introduced by the high impedance of via structures and the parasitic effects of via stubs are significant at mmWave. Stub reduction and additional matching are usually required to compensate, with the performance verified using full 3D electromagnetic (EM) simulation. Manufacturing tolerances of all the parameters should be considered early in design.

In many mmWave radars where the frequencies are higher than 60 GHz, the design must prevent radiation from the via structures. A dense ring of ground vias is usually placed around the signal via to provide a ground shield, containing the EM fields inside a quasi-coaxial structure and minimizing radiation loss. However, these ground vias can short the trace and block



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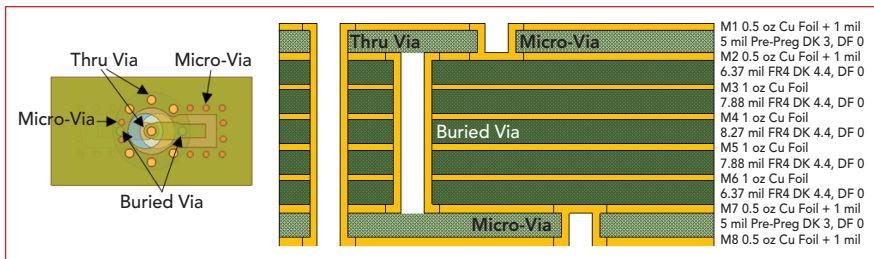
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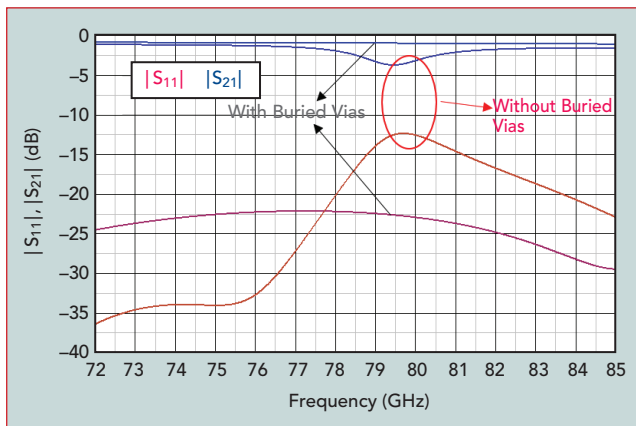


▲ Fig. 8 Via structure (left) for a 76 to 81 GHz layer transition and associated PCB stackup (right).

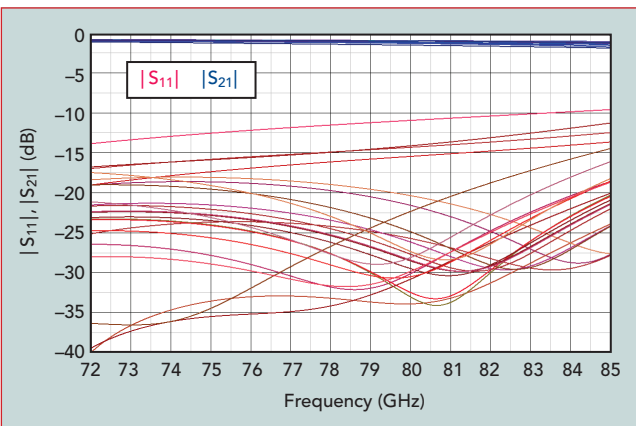
the signal routing in and out of the center signal via.

Figure 8 shows a via structure and its PCB stackup that conducts 76 to 81 GHz signals from the bottom to top layers in an automotive radar. Six plated through holes surrounding the center signal via serve as ground vias. However, they do not provide enough shielding at the upper frequencies, requiring two additional buried vias to close the gap while not shorting the traces. If the buried vias are removed, the insertion loss and return loss degrade significantly (see **Figure 9**). The tolerance study of the via transition is shown in **Figure 10**. It includes the manufacturing tolerances of etching, via registration, via diameter and variation of the dielectric material thickness and dielectric constant. Tolerance studies help ensure the RF performance meets system requirements considering all the manufacturing variability.

As discussed, buried vias require additional lamination, drilling and plating, and these additional processes can significantly increase manufacturing cost. A surface mountable (SMT) crossover component can be applied to a single lamination board to achieve the same



▲ Fig. 9 Buried via insertion loss and return loss comparison.



▲ Fig. 10 Tolerance study of the layer transition using buried vias.

results, reducing manufacturing complexity (see **Figure 11**). In this 76 to 81 GHz automotive radar design, only plated through hole vias and micro-vias are used in a common, single lamination stackup. The center signal via and surrounding ground vias are all plated through holes, and micro-vias are placed around the trace for the grounded coplanar waveguide (GCPW) lines. The isolated signal via pad and the end of the GCPW line are not connected by the routings on the PCB; they are bridged together by an SMT crossover component. Mounting the crossover on both top layer



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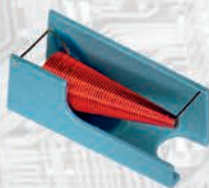
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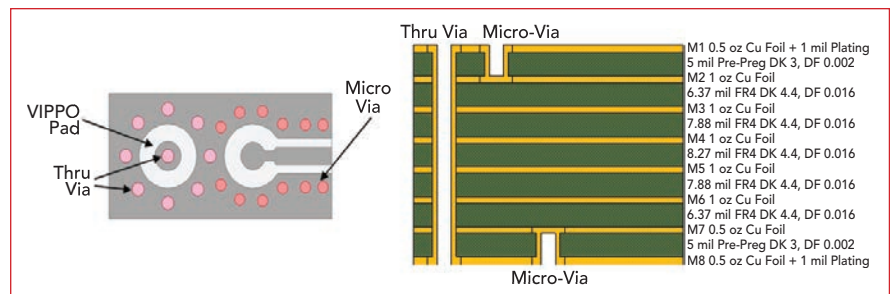
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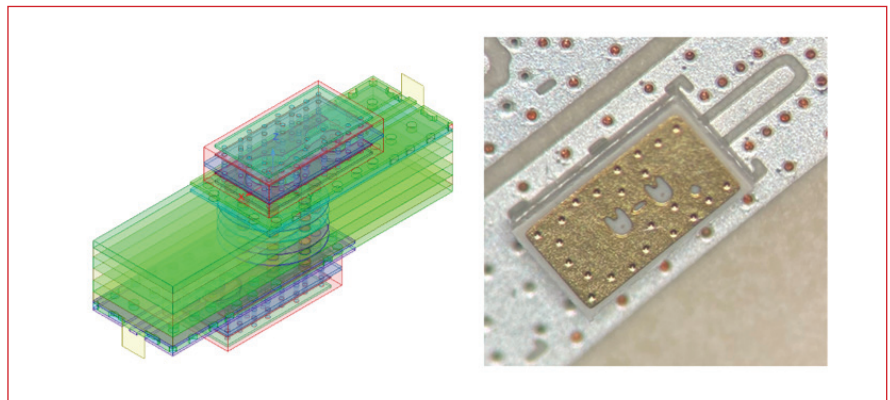
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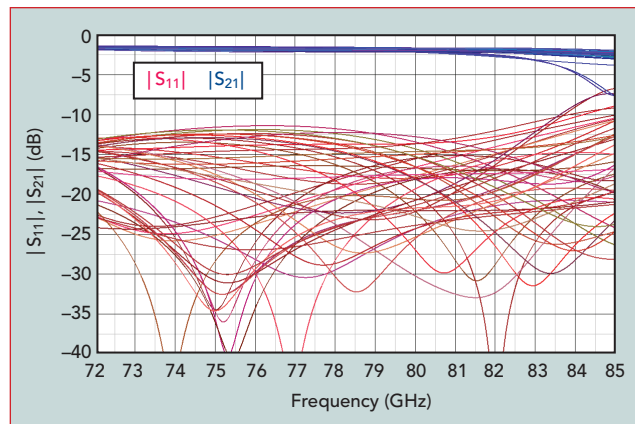
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▲ Fig. 11 Layout (left) and simplified PCB stackup (right) of layer transition using SMT crossover component.



▲ Fig. 12 Isometric view (left) and photo (right) of the layer transition using a crossover component.



▲ Fig. 13 Tolerance analysis of the layer transition using the crossover component.

and bottom layer, the signal is conducted from the GCPW line on the bottom layer to the GCPW line on the top (see Figure 12). The dimensions of the crossover are about 80 x 50 mil, and the crossover fits nicely with a 10 mil, 50 Ω GCPW line, commonly used for these applications. Since the crossover uses similar mmWave grade PCB substrates and the same multilayer PCB manufacturing processes, the SMT component approach can achieve the same performance and manufacturing process variation as a matched

via solution (compare Figure 13 with Figure 10). If a PCB has a low density of such signal transitions, the component solution may offset the added component cost by reducing the board manufacturing cost and yielding an overall price advantage.

SUMMARY

The rapid growth of mmWave applications has created a growing demand for high performance, multilayer PCBs containing mmWave circuitry. Today's mmWave design requirements can exceed PCB material and process capabilities, as relatively small variations in raw materials and manufacturing processes can degrade the performance of mmWave designs. By incorporating these material and process variations in the design, the desired performance, repeatability and cost in production can be achieved. ■



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Model No.	Freq (GHz)	Gain (dB) MIN	Noise Figure (dB)	Power-out @ P1-dB	3rd Order ICP	VSWR
CA01-2110	0.5-1.0	28	1.0 MAX, 0.7 TYP	+10 MIN	+20 dBm	2.0:1
CA12-2110	1.0-2.0	30	1.0 MAX, 0.7 TYP	+10 MIN	+20 dBm	2.0:1
CA24-2111	2.0-4.0	29	1.1 MAX, 0.95 TYP	+10 MIN	+20 dBm	2.0:1
CA48-2111	4.0-8.0	29	1.3 MAX, 1.0 TYP	+10 MIN	+20 dBm	2.0:1
CA812-3111	8.0-12.0	27	1.6 MAX, 1.4 TYP	+10 MIN	+20 dBm	2.0:1
CA1218-4111	12.0-18.0	25	1.9 MAX, 1.7 TYP	+10 MIN	+20 dBm	2.0:1
CA1826-2110	18.0-26.5	32	3.0 MAX, 2.5 TYP	+10 MIN	+20 dBm	2.0:1

NARROW BAND LOW NOISE AND MEDIUM POWER AMPLIFIERS

CA01-2111	0.4-0.5	28	0.6 MAX, 0.4 TYP	+10 MIN	+20 dBm	2.0:1
CA01-2113	0.8-1.0	28	0.6 MAX, 0.4 TYP	+10 MIN	+20 dBm	2.0:1
CA12-3117	1.2-1.6	25	0.6 MAX, 0.4 TYP	+10 MIN	+20 dBm	2.0:1
CA23-3111	2.2-2.4	30	0.6 MAX, 0.45 TYP	+10 MIN	+20 dBm	2.0:1
CA23-3116	2.7-2.9	29	0.7 MAX, 0.5 TYP	+10 MIN	+20 dBm	2.0:1
CA34-2110	3.7-4.2	28	1.0 MAX, 0.5 TYP	+10 MIN	+20 dBm	2.0:1
CA56-3110	5.4-5.9	40	1.0 MAX, 0.5 TYP	+10 MIN	+20 dBm	2.0:1
CA78-4110	7.25-7.75	32	1.2 MAX, 1.0 TYP	+10 MIN	+20 dBm	2.0:1
CA910-3110	9.0-10.6	25	1.4 MAX, 1.2 TYP	+10 MIN	+20 dBm	2.0:1
CA1315-3110	13.75-15.4	25	1.6 MAX, 1.4 TYP	+10 MIN	+20 dBm	2.0:1
CA12-3114	1.35-1.85	30	4.0 MAX, 3.0 TYP	+33 MIN	+41 dBm	2.0:1
CA34-6116	3.1-3.5	40	4.5 MAX, 3.5 TYP	+35 MIN	+43 dBm	2.0:1
CA56-5114	5.9-6.4	30	5.0 MAX, 4.0 TYP	+30 MIN	+40 dBm	2.0:1
CA812-6115	8.0-12.0	30	4.5 MAX, 3.5 TYP	+30 MIN	+40 dBm	2.0:1
CA812-6116	8.0-12.0	30	5.0 MAX, 4.0 TYP	+33 MIN	+41 dBm	2.0:1
CA1213-7110	12.2-13.25	28	6.0 MAX, 5.5 TYP	+33 MIN	+42 dBm	2.0:1
CA1415-7110	14.0-15.0	30	5.0 MAX, 4.0 TYP	+30 MIN	+40 dBm	2.0:1
CA1722-4110	17.0-22.0	25	3.5 MAX, 2.8 TYP	+21 MIN	+31 dBm	2.0:1

ULTRA-BROADBAND & MULTI-OCTAVE BAND AMPLIFIERS

Model No.	Freq (GHz)	Gain (dB) MIN	Noise Figure (dB)	Power-out @ P1-dB	3rd Order ICP	VSWR
CA0102-3111	0.1-2.0	28	1.6 Max, 1.2 TYP	+10 MIN	+20 dBm	2.0:1
CA0106-3111	0.1-6.0	28	1.9 Max, 1.5 TYP	+10 MIN	+20 dBm	2.0:1
CA0108-3110	0.1-8.0	26	2.2 Max, 1.8 TYP	+10 MIN	+20 dBm	2.0:1
CA0108-4112	0.1-8.0	32	3.0 MAX, 1.8 TYP	+22 MIN	+32 dBm	2.0:1
CA02-3112	0.5-2.0	36	4.5 MAX, 2.5 TYP	+30 MIN	+40 dBm	2.0:1
CA26-3110	2.0-6.0	26	2.0 MAX, 1.5 TYP	+10 MIN	+20 dBm	2.0:1
CA26-4114	2.0-6.0	22	5.0 MAX, 3.5 TYP	+30 MIN	+40 dBm	2.0:1
CA618-4112	6.0-18.0	25	5.0 MAX, 3.5 TYP	+23 MIN	+33 dBm	2.0:1
CA618-6114	6.0-18.0	35	5.0 MAX, 3.5 TYP	+30 MIN	+40 dBm	2.0:1
CA218-4116	2.0-18.0	30	3.5 MAX, 2.8 TYP	+10 MIN	+20 dBm	2.0:1
CA218-4110	2.0-18.0	30	5.0 MAX, 3.5 TYP	+20 MIN	+30 dBm	2.0:1
CA218-4112	2.0-18.0	29	5.0 MAX, 3.5 TYP	+24 MIN	+34 dBm	2.0:1

LIMITING AMPLIFIERS

Model No.	Freq (GHz)	Input Dynamic Range	Output Power Range Psat	Power Flatness dB	VSWR
CLA24-4001	2.0-4.0	-28 to +10 dBm	+7 to +11 dBm	+/- 1.5 MAX	2.0:1
CLA26-8001	2.0-6.0	-50 to +20 dBm	+14 to +18 dBm	+/- 1.5 MAX	2.0:1
CLA712-5001	7.0-12.4	-21 to +10 dBm	+14 to +19 dBm	+/- 1.5 MAX	2.0:1
CLA618-1201	6.0-18.0	-50 to +20 dBm	+14 to +19 dBm	+/- 1.5 MAX	2.0:1

AMPLIFIERS WITH INTEGRATED GAIN ATTENUATION

Model No.	Freq (GHz)	Gain (dB) MIN	Noise Figure (dB)	Power-out @ P1-dB	Gain Attenuation Range	VSWR
CA001-2511A	0.025-0.150	21	5.0 MAX, 3.5 TYP	+12 MIN	30 dB MIN	2.0:1
CA05-3110A	0.5-5.5	23	2.5 MAX, 1.5 TYP	+18 MIN	20 dB MIN	2.0:1
CA56-3110A	5.85-6.425	28	2.5 MAX, 1.5 TYP	+16 MIN	22 dB MIN	1.8:1
CA612-4110A	6.0-12.0	24	2.5 MAX, 1.5 TYP	+12 MIN	15 dB MIN	1.9:1
CA1315-4110A	13.75-15.4	25	2.2 MAX, 1.6 TYP	+16 MIN	20 dB MIN	1.8:1
CA1518-4110A	15.0-18.0	30	3.0 MAX, 2.0 TYP	+18 MIN	20 dB MIN	1.85:1

LOW FREQUENCY AMPLIFIERS

Model No.	Freq (GHz)	Gain (dB) MIN	Noise Figure dB	Power-out @ P1-dB	3rd Order ICP	VSWR
CA001-2110	0.01-0.10	18	4.0 MAX, 2.2 TYP	+10 MIN	+20 dBm	2.0:1
CA001-2211	0.04-0.15	24	3.5 MAX, 2.2 TYP	+13 MIN	+23 dBm	2.0:1
CA001-2215	0.04-0.15	23	4.0 MAX, 2.2 TYP	+23 MIN	+33 dBm	2.0:1
CA001-3113	0.01-1.0	28	4.0 MAX, 2.8 TYP	+17 MIN	+27 dBm	2.0:1
CA002-3114	0.01-2.0	27	4.0 MAX, 2.8 TYP	+20 MIN	+30 dBm	2.0:1
CA003-3116	0.01-3.0	18	4.0 MAX, 2.8 TYP	+25 MIN	+35 dBm	2.0:1
CA004-3112	0.01-4.0	32	4.0 MAX, 2.8 TYP	+15 MIN	+25 dBm	2.0:1

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No Manning Required Ship (NOMARS) Program to Build, Test, Demonstrate First Ship

The Defense Advanced Research Projects Agency (DARPA) is moving into Phase 2 of the NOMARS program, which seeks to build and demonstrate a revolutionary new medium unmanned surface vessel (MUSV) that can go to sea and perform missions with unprecedented reliability and availability, while carrying a significant payload. The agency selected Serco Inc.'s design to move forward at the conclusion of Phase 1.

NOMARS took a clean-sheet approach to ship design, holding firmly to the requirement that there will never be a human on board the vessel while it is at sea—including during underway replenishment events. By eliminating all constraints and requirements associated with humans, NOMARS opened the design space to novel ship configurations and capabilities that could never be considered for crewed vessels.

In Phase 1, Serco developed a new Design Space Exploration (DSX) toolset that can evaluate spaces with a variety of parameters and outputs millions of ship designs to meet a diverse set of performance objectives and constraints. Serco used their DSX tool to create a set of ship designs ranging from 170-270 metric tons, then refined those into a single ship for the preliminary design review, dubbed Defiant. In Phase 2, Serco will finalize ship design, build the ship and work through a series of rigorous testing activities before taking it to sea for a three-month demonstration event. Serco is working with Beier Integrated Systems LLC, Caterpillar, DRS Naval Power Systems Inc., ICE FLOE LLC (dba Nichols Brothers Boat Builders), Metron Inc., Serco Inc., Submergence Group LLC and Thrustmaster of Texas Inc. on the project.

Defiant will be the first of its kind. The 210-metric ton MUSV-class ship aims to maximize performance, reliability and maintenance efficiency while still carrying significant payload at tactically useful ranges. The goal is to achieve ultra-reliability objectives by integrating distributed hybrid power generation, podded propul-

sors and high capacity batteries. A key philosophy of NOMARS is "graceful degradation," which allows individual equipment to fail over time by having enough system-level redundancy to meet full system requirements at speeds of at least 15 knots after one year at sea. The major system components of the selected design are modularized, so repairs can be conducted with equipment typically found in yacht-yards worldwide. This maintenance philosophy supports rapid turnaround, allowing the ships to spend a majority of their lifetime at sea performing missions.

Two-for-Two: Hypersonic Missile Passes Second Consecutive Test

A hypersonic cruise missile co-developed by Raytheon Technologies has passed its second flight test in a row—an important milestone in the U.S. Department of Defense's plan to field weapons that travel faster than 5x the speed of sound.

The test, conducted in July 2022, featured a Hypersonic Air-breathing Weapon Concept (HAWC), with minor improvements informed by its earlier successful test in September 2021. Its performance in the most recent test—it dropped from an aircraft and accelerated beyond Mach 5—met the predictions of the company's data models.

The HAWC program is a joint effort of DARPA and U.S. Air Force.

The HAWC missile takes in oxygen around it for propulsion. Northrop Grumman designed its scramjet combustor and a portion of the flow path. The system represents one way Raytheon Technologies is teaming across industry to accelerate hypersonic advances, bringing proven technology together with cutting-edge developments in thermal management, propulsion and sensing.

Hypersonic weapons demand novel design solutions because their speed and maneuverability create challenging operating environments. To develop and validate the system quickly, the company has used digital engineering, specifically modeling and simulation, along with ground testing.

Digital engineering "helps us find new materials, manufacturing processes and aerodynamic shapes that can withstand extreme conditions while delivering required performance," said Wes Kremer, president of



Defiant (Source: DARPA)



HAWC (Source: Raytheon Technologies)

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The latest test follows the Raytheon Technologies/Northrop Grumman team's first-ever flight test of a HAWC missile in 2021. But countless tests have taken place in the digital world, gleaned valuable data used to help forecast real-world performance. These digital models, based on real-world flight data, are being used to accurately predict and increase performance as the weapon concept matures.

The latest tests put the companies on track to deliver an operational prototype system to the U.S. Department of Defense.

Leap-Forward Technology for Next-Gen Radar and Communications Systems

DARPA has awarded BAE Systems' FAST Labs™ research and development organization a \$17.5 million contract for the Generating RF with Photonic Oscillators for Low Noise (GRYPHON) program. The breakthrough technology developed through the program could enable an unprecedented combination of low noise, compact size and frequency agility for next-generation airborne sens-

ing and communications capabilities.

Electronic oscillators are the vital technology driving virtually all microelectronic systems. Currently, high performance requires large, power-hungry systems—the size of a mini-fridge. BAE Systems' approach will maintain or improve performance while reducing the system to the size of a quarter.

BAE Systems' innovative solution combines the efficiency and agility of digital electronics, and the bandwidth and stability of photonics to deliver precision microwave sources in an unprecedentedly small form factor. This drastically improves size, weight, power and cost and allows this next-generation, mission critical technology to be deployed on smaller platforms and creates a new category of systems.

Work on the program, which is part of BAE Systems' advanced electronics portfolio, includes collaboration with subcontractor GenXComm. GenXComm is helping lead the photonics subsystem development for BAE Systems' work on the GRYPHON program and specializes in the development of advanced microphotonics for RF signal processing to enable high throughput, ultra-low latency, interference free wireless mesh networks. GenXComm was introduced to FAST Labs through the technology scouting arm of the organization.



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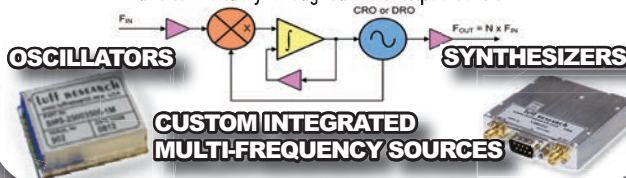


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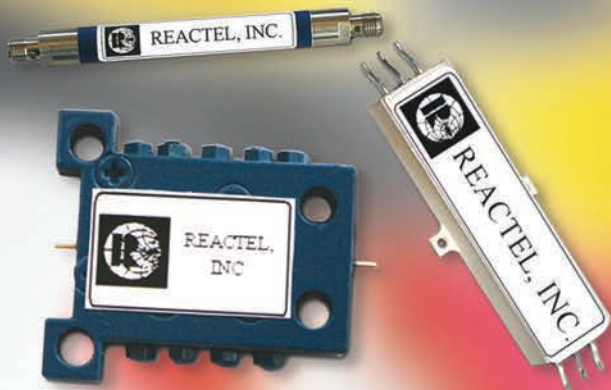


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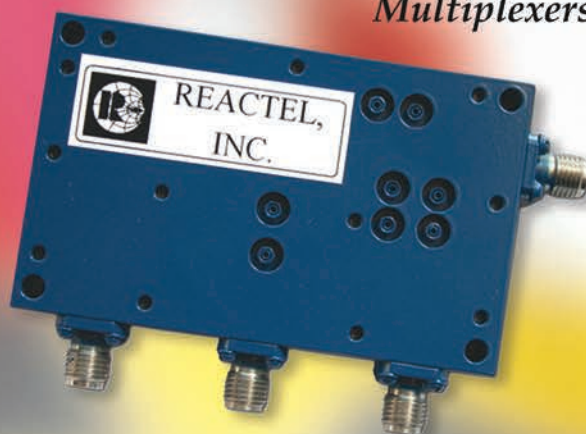
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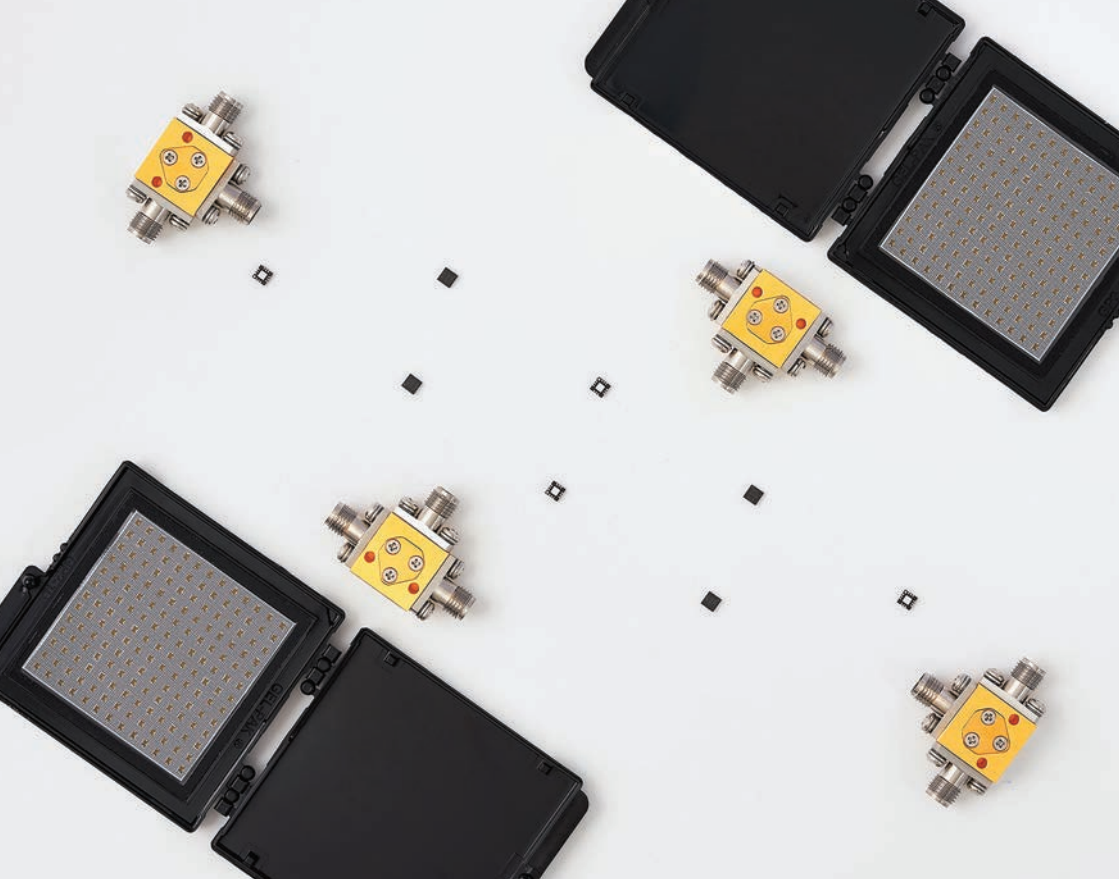


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Harnessing the THz Spectrum for Amazing Possibilities

The terahertz (THz) realm of the radio spectrum presents tantalizing possibilities (and challenges) for mobile communications and a panoply of novel applications—from see-in-the-dark sensors and revolutionary imaging and communications technologies to Tricorder-like medical devices. Realizing the potential of this underused region of the electromagnetic spectrum will require a solid foundation in THz device modeling and measurement.

NYU WIRELESS, an innovative academic research center at the NYU Tandon School of Engineering with a focus on 5G and beyond, is poised to lay the groundwork for that future, thanks to funding from the National Science Foundation for a new THz measurement facility. The \$3 million award from the 2022 NSF MRI Program will help NYU and its collaborators, the University of Colorado at Boulder, University of Nebraska–Lincoln and Florida International University pioneer basic measurements of devices, circuits, materials and radio propagation channels at the highest reaches of the radio spectrum.

The award, augmented by additional support from NYU bringing the total to over \$4.3 million, will allow NYU WIRELESS to purchase new cutting-edge equipment to study propagation and channel modeling, as well as RFIC on-chip measurement capabilities up to 500 GHz, according to NYU WIRELESS Founding Director Theodore (Ted) S. Rappaport, Tandon's David Lee/Ernst Weber Professor of Electrical Engineering and principal investigator on the new NSF award. The latter capability of this new THz measurement facility aligns with the recent bipartisan CHIPS-Plus Act legislation that includes over \$52 billion in subsidies for expanding semiconductor manufacturing in the U.S.

The program allows for the center to lend the three partner institutions THz components for remote field measurements for wireless communications, propagation and sensing. Additionally, evolving semiconductors and ICs, as well as the next-generation electronics based on layered materials (e.g., graphene), will be measured at THz bands using the RFIC probe station.



Antenna Tower (Source: NYU)

The THz measurement facility will host a website explaining available equipment, tutorials for learning how to use the facility and a repository of measurement results, metrology approaches and recent research results. It will include simulators, measurement studies, calibration results, student and collaborator activities, sponsor and vendor activities, equipment user notes and K-12 outreach events.

5G Time Critical Services to Boost Productivity and Efficiency of Industrial Operations

Modern 5G networks have introduced technologies such as ultra-reliable low latency communication (URLLC) and time sensitive networking (TSN) support to address a host of time critical networking needs. 5G Americas announced the release of its latest white paper covering time critical services in 5G networks entitled, "Understanding 5G and Time Critical Services."

Chris Pearson, president of 5G Americas said, "The continued advancements of fifth generation of wireless cellular standards and networks will address new enterprise and industrial use cases. These complex use cases often require data delivery within a specified time duration with a high degree of guaranteed reliability."

According to the white paper, time critical services require the services' clients and servers across the network to be strictly synchronized, and its underlying communication network to be ultra-reliable and strictly latency-bounded. URLLC and TSN features in 5G will help support an array of use cases spanning across automotive, transportation, healthcare, education, media production, forestry, public safety, banking, utilities and more.

Support for time critical services over 5G networks have been incorporated in various enhancements in Releases 16 and 17. The white paper describes how these technologies are impacting legacy networks based on GNSS that have traditionally provided required timing accuracy, as well as the Institute of Electrical and Electronics Engineers IEEE 802.1 TSN standard that is becoming the converged networking technology for factories to enable deterministic and low latency communication.

"Understanding 5G and Time Critical Services" explores the following key topics:

- Key use cases and requirements
- Technology enablers in 5G Release 16 and 17
- 5G architecture supporting time synchronization, IEEE TSN and application function
- Requested time sensitive communication
- Timing service resiliency
- URLLC

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- Time synchronization accuracy and services
 - Security of timing as a service over 5G.
- Engineers from Intel and Qualcomm led the working group that authored the paper.

5G Private Networks are Essential for Industrial Automation, Robotics and Augmented Reality

Network upgrades can underpin the efforts of manufacturers to automate quality assurance processes, deploy autonomous mobile robots inside the facility and upskill employees using augmented reality. Lower latency and support for time sensitive networking afforded by a 5G network can further enable wireless process automation for robotics use cases and increase bandwidth support for data-heavy applications, such as video analytics. According to new research from ABI Research, in 2030, manufacturing and industrial firms worldwide will have more than 49 million 5G connections inside their facilities, generating \$2.4 billion in global connections revenue for suppliers.

"Progressive advancements to network performance (from Wi-Fi to Long Term Evolution (LTE), and from LTE to

5G) can underpin improvements to customers' operations. But to maximize the benefits to their operations, customers will need to invest in ancillary technologies, such as edge networking, data management and data analytics to accelerate data collection and create a digital thread," said Michael Lerner, industrial and manufacturing research director at ABI Research.

However, a lack of 5G industrial devices has stalled manufacturers' interest in 5G private wireless. In turn, the lack of enthusiasm has discouraged hardware suppliers from creating the necessary devices. As a result of the state of flux, equipment vendors, such as Nokia, have launched converged devices supporting Wi-Fi, LTE and 5G connectivity.

Suppliers need to showcase the attributes of a 5G network and prove how a 5G network can upgrade operations. "The lack of 5G devices is a genuine drag on adoption, but suppliers (telcos such as Nokia, Ericsson, NTT), information technology providers (HPE, DXC, Dell Technologies), operational technology specialists (Bosch, Siemens, Honeywell) and system integrators (such as Accenture and Deloitte) should be working with prospective customers to educate them today about 5G's potential," Lerner concluded.

These findings are from ABI Research's 5G Private Wireless in Manufacturing market update report.

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Mini-modules are currently available in standard waveguide bands for 26GHz to 1.1THz with higher frequency bands under development.

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Dynamic Range (BW=10Hz, dB, typ) (BW=10Hz, dB, min)	120 110	120 105	120 110	120 110	120 110	120 110	120 110	120 110	115 110	115 105	100 80	110 100	100 80	95 75
Magnitude Stability (±dB)	0.15	0.15	0.10	0.10	0.10	0.15	0.25	0.25	0.3	0.3	0.5	0.5	0.4	0.5
Phase Stability (±deg)	2	2	1.5	1.5	1.5	2	4	4	4	6	6	6	4	6
Test Port Power (dBm)	13	13	13	18	18	16	13	6	4	1	-10	-3	-16	-23



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Around the Circuit

Barbara Walsh, Multimedia Staff Editor

MERGERS & ACQUISITIONS

Renesas Electronics Corp. announced that it has entered into a definitive agreement to acquire **Steradian Semiconductors Private Limited**, a fabless semiconductor company based in Bengaluru, India, that provides 4D imaging radar solutions, in an all-cash transaction. The acquisition is expected to close by the end of 2022, subject to customary closing conditions. The acquisition of Steradian's radar technology will enable Renesas to extend its reach in the radar market and boost its automotive and industrial sensing solution offerings.

Naprotek LLC., a provider of high reliability, quick-turn electronics manufacturing, has completed the acquisition of **MicroFab Inc.**, a privately held company in Manchester, N.H. This acquisition is a strategic element of Naprotek's continued expansion in RF products, services and solutions. Naprotek now offers customers an array of custom build-to-print thin film products, supported by enhanced capabilities and a wider spectrum of thin film technologies. The business and entire MicroFab team will be integrated into the East Coast operations at SemiGen, a Naprotek Company.

COLLABORATIONS

Modelithics and **MACOM Technology Solutions Inc.** announced the release of new models for three MACOM components: the MAPD-011062 power divider, the MACP-011088 bi-directional coupler and the MABA-011125 balun. Each model is a substrate selectable S-parameter data model valid through 50 GHz. The new models are available within the Modelithics COMPLETE Library™ as well as the Modelithics mmWave & 5G Library. Both the MAPD-011062 power divider and the MABA-011125 balun come in a 3-mm, 16-lead QFN package, while the MACP-011088 bi-directional coupler comes in a 4-mm, 24-lead QFN package.

Cadence Design Systems Inc. announced that it has collaborated with **GlobalFoundries** to accelerate 5G and mobile design innovation through the delivery of the Cadence® RF and mmWave flow for the GF 22FDX platform. The Cadence full-flow RF solution was used to design and tape out a 28 GHz 5G mmWave IC on the GF® 22FDX platform and design an integrated antenna as a complete system-in-package solution. The mmWave IC design was simulated with the Cadence AWR® Visual System Simulator™ (VSS)—using the combined Rohde & Schwarz signal creation and analysis tools within the R&S® VSESIM-VSS supporting 5G NR—and showed a high correlation to Si measurements and lab testing performed by the German institute, Fraunhofer IIS/EAS.

Qualcomm Technologies Inc. and **ZTE** announced the fastest 5G mmWave standalone (SA) data connection,

achieving impressive results in two scenarios: nearly 7 Gbps peak rate for downlink and 2.1 Gbps for uplink. 5G SA mmWave allows for the deployment of 5G mmWave networks and devices without using an anchor on LTE or sub-6 GHz spectrum. This gives operators more flexibility to deliver wireless fiber broadband access with multi-Gigabit speeds and ultra-low latency to residential and commercial customers. Use of mmWave SA without an anchor also enables green field fixed wireless access deployments for all use-cases.

Thorium Space, a company in the advanced satellite communication systems sector, has officially started work on a joint project in cooperation with **Teledyne e2v Semiconductors**, a global company in the field of advanced technologies used in the aerospace and defence sector. The fact that such a recognized company with a global reach decided to cooperate with an emerging Polish company is indicative of the leading-edge solution proposed by Thorium Space. Work will focus on the definition and development of state-of-the-art key elements of an advanced communication payload that will offer more efficient use of the spectrum and satellite payload resources.

Airgain, a global provider of wireless connectivity solutions, including embedded components, external antennas and integrated systems, has announced a collaboration with **The Fraunhofer Heinrich Hertz Institute (HHI)**, a world leader in the development of mobile and fixed broadband communication networks and multimedia systems based in Berlin, Germany. Connectivity without disruption for mobile and fixed wireless access usage is a major goal of all operators and end customers. This collaboration focuses on developing the critical building blocks of wireless systems and intelligent networks to improve the user experience for both operators and customers.

NEW STARTS

Times Microwave Systems is expanding its Netherlands master distribution hub by 50 percent to manage growing demand for its products and services in Europe. The expansion will add 600 m² (6,458 ft²) to its current 1,200 m² (12,916 ft²) warehouse in Houten, the Netherlands, to support increasing volume of shipments moving through the facility. The additional space will allow Times Microwave Systems' Netherlands operation to establish new cross-docking processes and consolidate shipments, optimizing efficiency and reducing freight costs to support continued business growth in the region.

CONTRACTS

Inmarsat Government announced that the **Defense Information Systems Agency** has awarded Inmarsat Government the **U.S. Navy Military Sealift Command** next-generation wideband follow-on contract for worldwide end-to-end commercial satellite communications services. An indefinite delivery, indefinite quantity contract, the ceiling value of the award is \$578 million over

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SDCHP-140	10 - 400	18.75	1	0.5 / 0.85	27 / 22	25
SBCHP-1100	10 - 1000	10	0.5	1.2 / 1.4	17 / 15	5
KBK-HP-1100	10 - 1000	10	0.5	1.2 / 1.4	17 / 15	5
KDK-HP-255	20 - 550	20	0.4	0.25 / 0.35	23 / 18	27.5
SDCHP-255	20 - 550	20	0.4	0.25 / 0.35	23 / 20	27.5
SDCHP-335	30 - 350	20.1	0.85	0.24 / 0.32	24 / 20	75
SDCHP-484	40 - 840	19.2	0.9	0.3 / 0.4	24 / 20	30
SCCHP-560	50 - 560	14.6	0.7	0.48 / 0.65	23 / 20	75
SCCHP-990	90 - 900	15.2	0.6	0.52 / 0.64	20 / 17	38.3
SBCHP-2080	200 - 800	12.3	0.7	0.64 / 0.80	24 / 18	48.3
SBCHP-2082	200 - 820	11.0	0.5	0.74 / 0.9	22 / 19	22.5
KDS-30-30-3	27 - 512	27.5	0.75	0.3 / 0.4	23 / 15	50
KDS-30-30	30 - 512	27.5	0.75	0.3 / 0.4	23 / 15	50
KBK-10-225	225 - 400	11	0.5	0.6 / 0.7	25 / 18	50
KBS-10-225	225 - 400	10.5	0.5	0.6 / 0.7	25 / 18	50
KDK-20-225	225 - 400	20	0.5	0.2 / 0.4	25 / 18	50
KDS-20-225	225 - 400	20	0.5	0.2 / 0.4	25 / 18	50
KEK-706H	500 - 2500	31.5	2.5	0.28 / 0.4	18 / 12	100
SCS-8012D	800 - 1200	20	0.6	0.22 / 0.25	22 / 18	100
KEK-704DH-2	850 - 1250	30	0.25	0.20 / 0.30	28 / 25	500
KEK-704H	850 - 960	30.5	0.25	0.08 / 0.20	38 / 30	500
SCS100800-10	1000 - 8000	10.5	2	1.2 / 1.8	8 / 5	25
SCS100800-16	1000 - 7800	16.8	2.8	0.7 / 1	14 / 5	25
SCS100800-20	1000 - 7800	20.5	2	0.4 / 0.75	12 / 5	25
SCS-1522B	1500 - 2200	10	--	0.65 / 0.75	23 / 18	100
SCS-1522D	1500 - 2200	20	--	0.32 / 0.38	23 / 20	100
SCS1701650-16	1500 - 15500	17	2.5	1 / 1.4	16 / 5	25
SCS1701650-20	1700 - 15000	21	2.5	0.9 / 1.3	10 / 7	25
SDC360440-10	3600 - 4400	8.6	0.25	0.7 / 1.4	18 / 10	10
SDC360440-20	3600 - 4400	19	0.25	0.7 / 1.2	16 / 10	10

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Around the Circuit

a 10-year period. Under the contract, Inmarsat Government will maintain and operate commercial communications infrastructure, which includes satellite systems, teleport services and terrestrial services.

The U.S. Navy has awarded **BAE Systems** a \$42.6 million contract for production of seven Network Tactical Common Data Link (NTCDL) systems. NTCDL enables the U.S. Navy to simultaneously transmit and receive real-time intelligence, surveillance and reconnaissance data from multiple sources and enables the exchange of command-and-control information over multiple data links. The systems will be installed on aircraft carriers and the new Constellation class frigates. The NTCDL system enhances situational awareness and tactical battlefield advantage through a real-time exchange of voice, data, imagery and full-motion video from a variety of sources: air, surface, subsurface and man-portable. BAE Systems' solution is a modular, scalable system, designed to increase link capacity and embrace waveform evolution.

Viasat Inc., a global communications company, announced it was awarded a \$99 million order for Multi-functional Information Distribution System (MIDS) Joint Tactical Radio System terminals from **U.S. Naval Information Warfare Systems Command (NAVWAR)** on behalf of the MIDS Program Office.

Mercury Systems Inc. announced it was awarded an \$8 million contract from a leading aerospace and defense company to design and develop video switching technology for an intelligence, surveillance and reconnaissance application for rotary-wing aircraft. The contract was received on April 1, 2022 with an estimated lifetime value of approximately \$25 million and is expected to be delivered over the next several quarters. As the volume of video captured by airborne platforms continues to rapidly increase, streamlining the video distribution process provides pilots with essential information more quickly, enabling them to focus on the mission at hand.

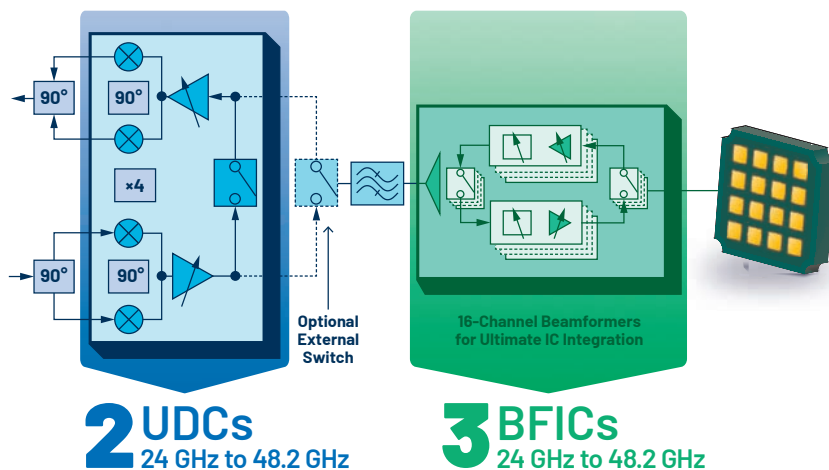
Akoustis Technologies Inc. announced that it has received a development order from a Fortune 100 Internet company for two new XBAW® driven diplexers for multiple applications. The two new Wi-Fi 7 diplexers are expected to enter pre-production in the second half of calendar 2023 and production in early calendar 2024. Each diplexer will ship with two XBAW® RF filters, an Akoustis designed switch and an integrated third-party antenna in Akoustis' proprietary new wafer-level packaging that is being developed in its Canandaigua, N.Y., manufacturing facility. The customer is targeting AR/VR, wearable and other applications both regionally and worldwide.

PEOPLE

Abrakon, an industry leader in passive components, has appointed **Tim Fedorov** as the company's new vice president of corporate development. Fedorov will focus on corporate development for Abracon, reporting

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ADMV1128 24 GHz to 29.5 GHz, 5G, Microwave Upconverter and Downconverter

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Around the Circuit



▲ Tim Fedorov

to Tony Roybal, president and CEO at the company's headquarters in Spicewood, Texas. Fedorov has over 20 years of technology and strategy experience spanning bio-medicals, semiconductors, telecommunications and industrial technologies.



▲ Grant Brown

Qorvo® announced the appointment of **Grant Brown** as chief financial officer, effective August 29, 2022. Brown was named interim chief financial officer on April 18, 2022, and previously served as Qorvo's vice president of Treasury.



▲ Ian Gresham

Anokiwave Inc. announced the latest addition to its executive leadership team with the appointment of **Ian Gresham** to the position of chief systems architect. Gresham will report directly to CEO Robert Donahue. As chief systems architect, Gresham's primary role is to drive the key performance indicators at the system level. In turn, he and his team are the main

drivers of the features and functions in their new product development.



▲ Thorsten Scheidler

Palomar Technologies, a global leader in delivering total process solutions for advanced photonics and microelectronic device packaging, announced the appointment of **Thorsten Scheidler** as the new managing director for its European operations effective October 1, 2022. Scheidler replaces Josef Schmidl who is retiring after 30+ years with Palomar

Technologies. Over his 30+ years with the company, Schmidl was instrumental in opening up the European market to Palomar semiconductor packaging equipment and building the market. He joined Hughes Aircraft in 1986 as a service and applications engineer.

REP APPOINTMENT

Quantic Wenzel, an industry leader in crystal oscillators, fixed-frequency systems, integrated microwave assemblies and synthesizers; announced that they have partnered with **Deh-Ron Ltd.** to support customers with mission-critical applications throughout Israel. Founded in 1982, Deh-Ron is headquartered in Tel Aviv-Yafo, Israel, and specializes in RF, microwave and mmWave solutions. Since 1978, Wenzel has defined the absolute state of the science in ultra-low phase noise crystal oscillators, a portfolio complemented by a range of advanced frequency sources and integrated microwave assemblies. Wenzel's oscillators and synthesizers are designed into mission-critical military, space and commercial applications.



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MMIC Filters' Time Has Come

Doug Jorgesen and Christopher Marki
Marki Microwave, Morgan Hill, Calif.

The outstanding fabrication tolerances and scalability of IC processes have made MMICs the technology of choice for nearly all planar microwave components, including amplifiers, mixers, switches, oscillators—even fully integrated transceivers. However, fixed filters have been untouched by the MMIC revolution due to outdated assumptions about performance and availability. In this article, we examine the filter landscape and explain why MMIC should be the technology platform of choice for many filter applications.

RF consumer markets have rapidly evolved over the last 10 to 15 years to offer enhanced data rates and connectivity while also supporting ever-increasing numbers of users and connected devices. A similar market evolution is taking place in the aerospace and defense, test and measurement and “new space” markets, where increased amounts of high frequency content are being processed and manipulated across significantly more users. Next-generation systems will increasingly support multichannel, multiband and multiple emitter architectures to improve performance and offer the ability to enable multipurpose missions, at the expense of a massive increase in overall channel count and total bandwidth. These channel counts are supported by high speed data converters, which enable high instantaneous bandwidth for both traditional super heterodyne and direct conversion receivers. The effect of increasing analog-to-digital converter (ADC) bandwidth is illustrated in **Figure 1**, which shows the changing filter requirements as more signal processing is performed digi-

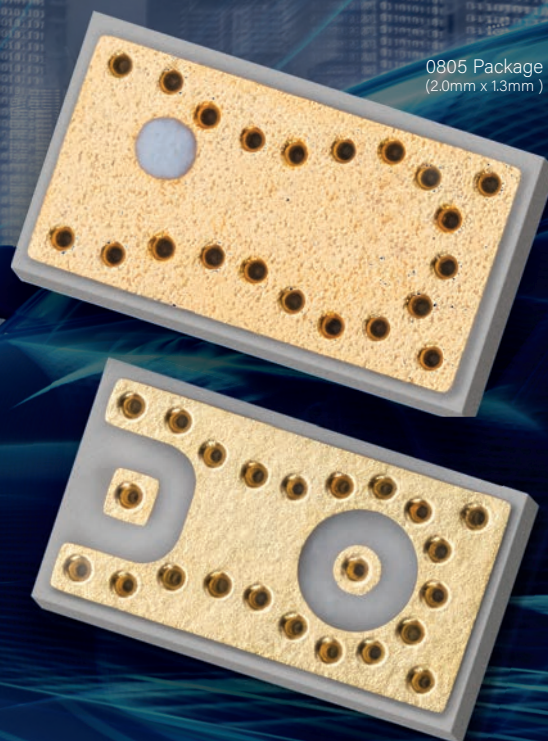
tally. Increasing ADC sampling rates enables narrowband filters to be implemented digitally, but the increasing channel count makes filter size more critical. These trends place incredible strain on the physical packaging of a particular solution, with the expectation that more channels and processing power be supported within the same, or sometimes smaller, footprints.

To support higher channel density, component solutions have generally followed an evolution that emphasizes smaller size and higher frequency. Additionally, many system blocks and sub-blocks have been combined through the development of single chip integrated solutions (typically Si ICs), through the novel packaging of multiple chips within a single package (called multi-chip modules) or through some combination of both Si and non-Si ICs inside the same package (usually referred to as “heterogeneous integration”). No doubt these trends will continue for the foreseeable future, and innovations will be necessary to further reduce the physical size of high frequency hardware.

Filters are commonly used to provide

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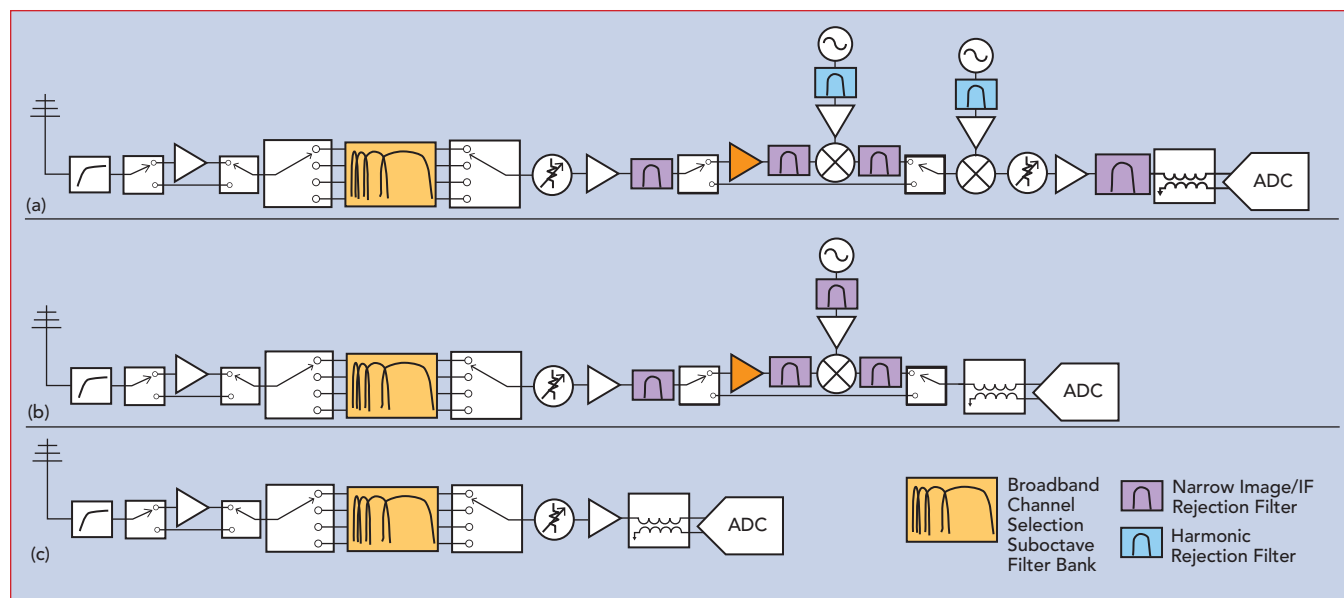


Fig. 1 Traditional superheterodyne receiver (a), superheterodyne receiver with digital down-conversion after the first IF stage (b) and direct conversion receiver (c).

channel or band selection and to clean up the spurious and unwanted signals or noise present in an analog signal chain. When it comes to miniaturization and improved channel density, filters are problematic be-

cause they consume much of a system's overall footprint. Given their ubiquity, it is curious to consider why filters remain the least evolved block in the system diagram. They often lack tunability or reconfigu-

rability, they are rarely integrated into a larger function block or package, they take up massive amounts of area and volume, they are susceptible to process variation causing lot-to-lot variability and they are often designed "in-house"—taking up valuable RF design resources.

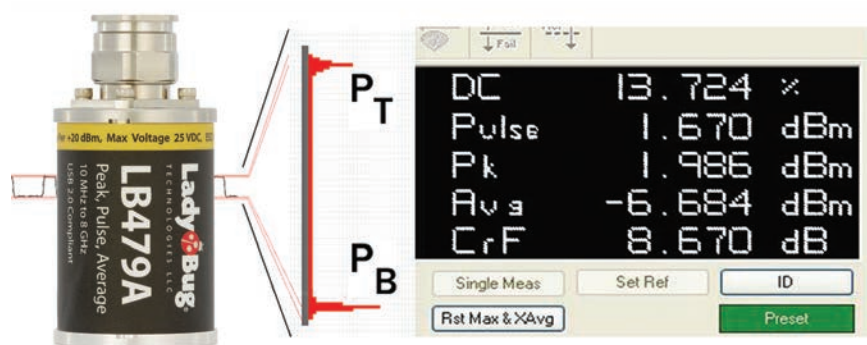
The demands on space and size have forced a reassessment of the performance tradeoffs of future filter solutions. The emerging trend is toward prioritizing reduced SWaP, scalability and rapid custom filter development over the traditional preferences of low loss (i.e., high Q-factor), high out-of-band rejection and high power. As converter bandwidths increase and more signal processing is performed digitally, less signal processing is required in the analog domain. Less processing means fewer converter stages—therefore, fewer spurs spaced farther apart. Some filter metrics, such as insertion loss for channel selection filters will always be important, but size, scalability and development time are becoming more dominant concerns for system architects.

A key challenge for high performance systems is that filters are typically custom designs based on the system frequency plan or some unique coexistence requirements. This creates a challenge when building a business case for low volume opportunities because costs can-

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not be offset by multiple customers. Further, filters are often needed immediately, as they are added or changed to solve a specific issue arising during development. This makes a rapid, reasonably priced, first-pass design success approach essential to solving a particular custom filter request.

Considering the above, we contend that future competitive filter technologies must satisfy the fol-

lowing critical metrics:

- Extremely small—at least 2× smaller than existing solutions and the smaller the better
- Rapid development cycle with modest cost and a first-pass success design flow
- Scalable, highly repeatable manufacturing approach
- Acceptable performance tradeoffs among insertion loss, filter order, rejection skirt, etc. to en-

able size reduction to meet the system need

- Operation from low GHz to >100 GHz to support all high frequency needs and preferably in a surface-mount package.

COMPARING FILTER TECHNOLOGIES

No one filter technology is ideal for all applications, and no one performance metric defines a filter technology (see **Figure 2**). Performing a general comparison of filter technologies is complicated because a filter design can be a tradeoff among many parameters. While Q is important for a given design, there is no single figure of merit to predict how well a filter technology will meet a specification.

At a basic level, the Q of the resonator and the order of the filter are the most important factors determining the center frequency insertion loss and rejection slope. However, a typical filter spec is defined by insertion loss across the passband instead of at the center frequency and rejection at a particular frequency instead of a rejection slope. To meet a real filter specification requires the design pay careful attention to the insertion loss at the edge of the passband and the rejection close to the passband. Therefore, comparing different filter technologies requires comparison of not only the available Q and realizable filter order, but also the flexibility to implement different design techniques, including agreement with simulation.

Common filter technologies used today include acoustic wave filters, cavity filters, lumped element filters and planar filters. In traditional space constrained, “low frequency” environments such as handsets, Wi-Fi and many other consumer products, surface acoustic wave and bulk acoustic wave filters are extensively used. They offer superb rejection, low loss and small form factor but are limited to ~1 W power handling and frequencies below ~8 GHz for applications that drive significant volume. For lower volume applications with more available board space, a lumped element filter can offer low cost and good perfor-

The advertisement features a dark blue background with a stylized white swoosh logo at the top. Below the logo, the text "NORDEN MILLIMETER" is displayed in a bold, sans-serif font. Underneath, the product types "RF Amplifiers, Multipliers, Converters, and Transceivers" are listed, followed by the frequency range "0.5 - 110 GHz". A central image shows three fighter jets in flight against a lighter blue sky. Below the jets, the text "Norden Millimeter combines extensive engineering and prototyping with efficient engineering to create RF products that address your military and commercial needs." is written. At the bottom, there is a photograph of a silver, rectangular RF component with the Norden Millimeter logo and name on its top surface. The contact information "Sales@NordenGroup.com", "530-719-4704", and "www.NordenGroup.com" is provided at the very bottom.

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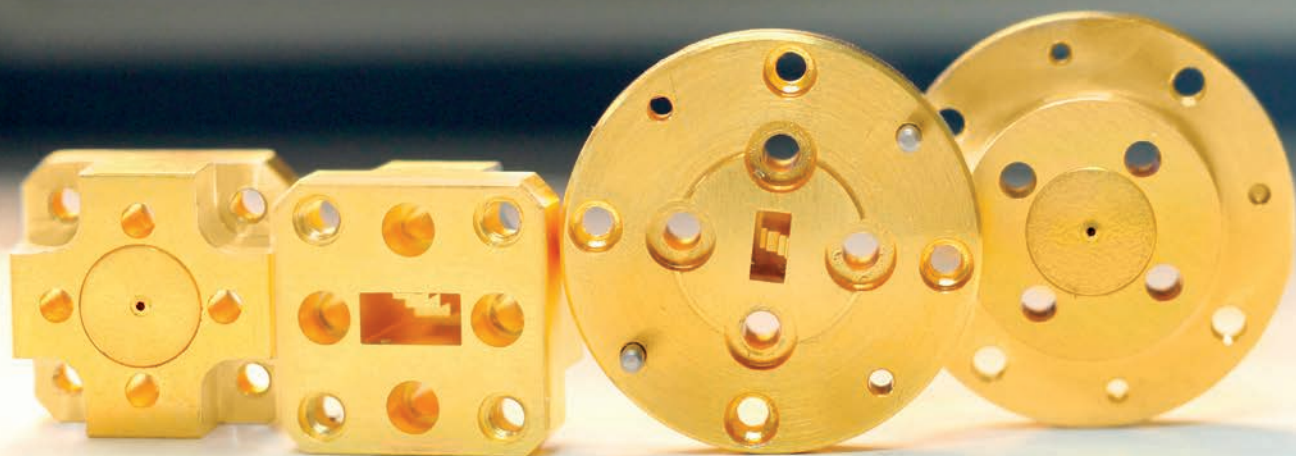
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mance below 6 GHz but has poor performance at microwave frequencies.

On the other end of the spectrum, cavity filters provide the ultimate in rejection with very low loss and high power handling at microwave frequencies but are physically large, require hand tuning and are costly at any volume. These are used broadly in high-power communications systems such as macro

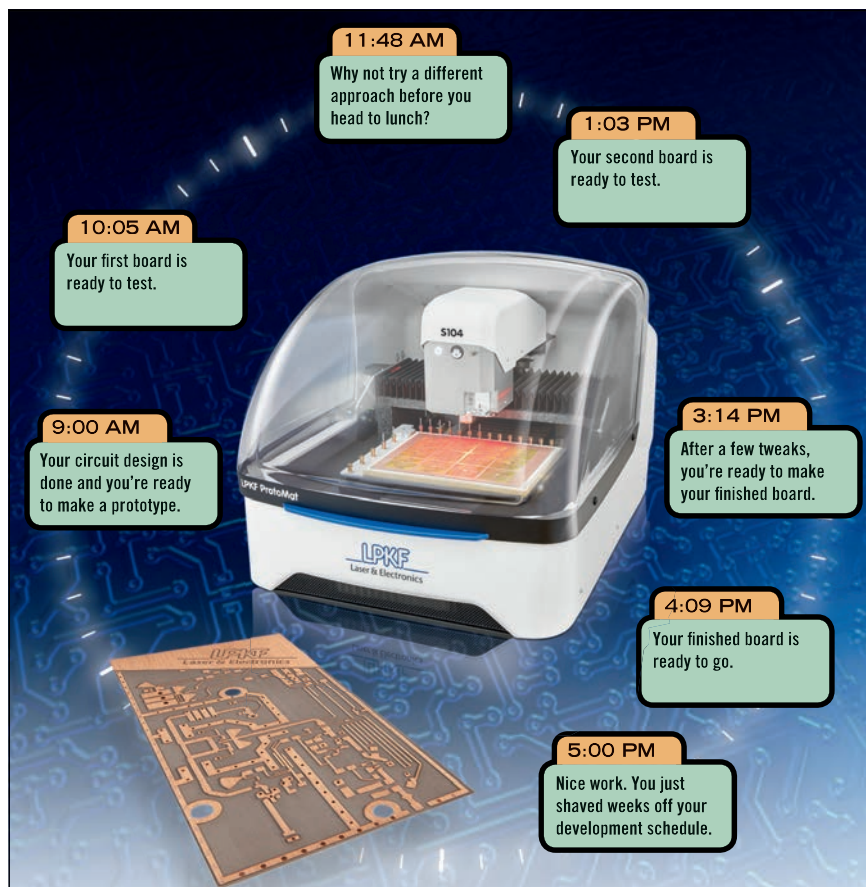
base stations for cellular networks. Between these extremes in size and cost is the class of filter that Marki and our customers use most frequently: planar circuit filters. Planar circuit filters implemented in MMIC technology offer an excellent tradeoff between electrical performance, size, development time, development cost and unit cost for broadband microwave systems (see **Table 1** for a comparison of five fil-

ter technologies). Marki is not tied to any fabrication technology, as we have the capability to design on laminate, thin film—ceramic, glass, sapphire and other exotic materials—or GaAs, what we call “MMIC filters.” While not traditionally considered for filter fabrication, MMIC offers the best combination of performance, cost and consistency.

A planar filter consists of a dielectric substrate with metal printed on top. The metal is patterned to electromagnetically couple resonators to yield a desired response. How this is done is the subject of countless textbooks and publications and is beyond the scope of this article. For an excellent overview of planar filter design, we recommend “Microstrip Filters for RF/Microwave Applications” by Jia-Sheng Hong. The art of planar filter design involves the careful choice of filter topology, resonator, circuit layout, optimization and tuning. A vast number of techniques are available to a filter designer; quickly narrowing the scope of options to compromise between size and performance is critical. While it takes only minutes to determine the best filter topology for a specification, it can often take several days of modeling and simulation to arrive at the final solution.

The design of a typical distributed planar filter is similar for the various fabrication methods (i.e., laminate, thin film including ceramic, glass, more exotics and MMIC) and largely requires the same software tools. Critical differences between the planar filter manufacturing methods include:

- Some fabrication processes support lumped and semi-lumped inductors and capacitors. The availability of these components impacts the variety of filter topologies that can be realized and strongly influences the achievable size.
- The dielectric and metal material properties and thicknesses vary among the processes. They are critical for determining the minimum size of a filter design and also dictate the available Q-factor and overall size of each resonator.
- The tolerances of the manufac-



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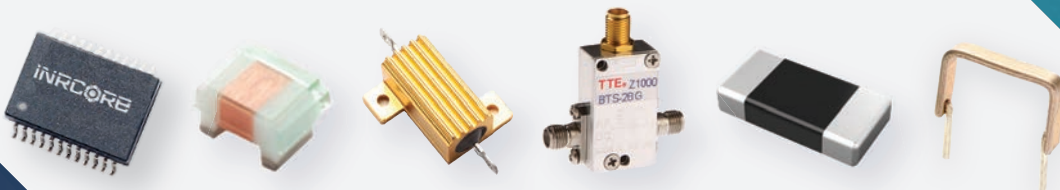
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turing processes can vary wildly. The tighter the tolerance, the better the filter repeatability from unit to unit and lot to lot. Tighter tolerance enables superior design flow for matching simulation and measurement—critical for first-pass design success.

MMIC FILTERS VS. LAMINATE

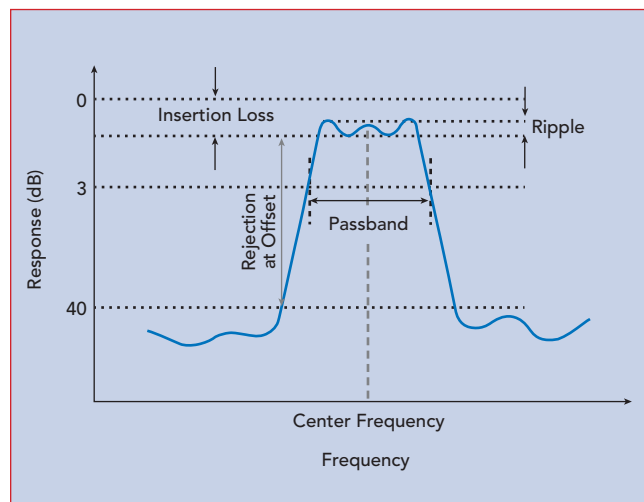
It is common practice to print filters in-situ on the circuit board that holds all the other components in an RF system. This do-it-yourself approach may seem practical and low-cost, but it introduces hidden costs and risks to system performance. These include:

Repeatability risk — While laminate filters are straightforward to design, the realistic manufacturing of laminate boards, especially multi-layer RF boards, is subject to routine variation in etching and lamination thickness. The typical etching tolerance of a laminate board is 25 μm , which translates to dimensional variation that will detune the filter. In some designs, errors of 2 to 3 percent in resonator frequency or coupling factor can be very problematic, and a poorly controlled laminate process can easily exceed 10 percent dimensional error in certain circumstances. A typical MMIC technology is two orders of magnitude more accurate with line and space accuracy measured in fractions of microns.

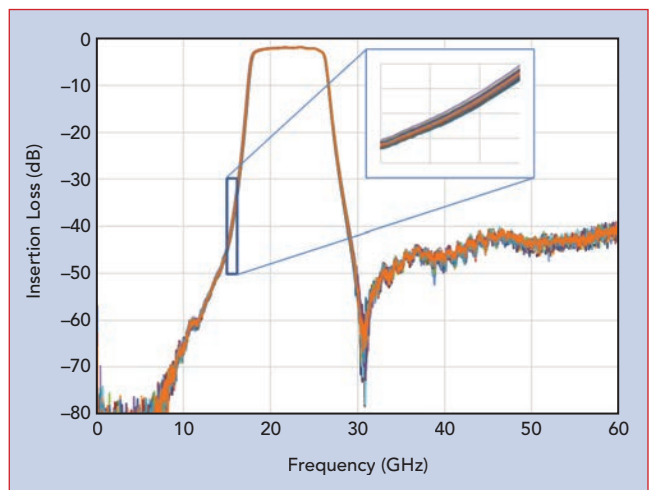
In-situ performance risk — The performance of a laminate filter is known to vary but, unlike a MMIC filter, it cannot be tested prior to assembly. A system must be completely assembled and found to fail a spec before the underperformance of the in-situ filter can be identified. This introduces significant cost and risk to a production design, as a completed board may be as expensive as 100 discrete filters.

Size risk — Due to the ~4x higher dielectric of GaAs compared to the most common laminates and the fine tolerance of MMIC fabrication,

Technology	MMIC	Thin Film	Laminate	Cavity	Lumped
Size	5	3	2	1	2
Power Handling	2	2	4	5	3
Performance					
< 10 GHz	3	3	3	5	5
10 – 20 GHz	3	3	4	5	2
20 – 50 GHz	4	3	3	4	1
50 – >100 GHz	4	N/A	N/A	3	1
Q Factor	2	3	3	5	4
Practical Filter Order	2 (< 9th Order)	3 (< 11th Order)	4 (<15th Order)	5	3
Narrowband Limit (% Bandwidth)	> 8	> 6	> 5	Any	Any
Transmission Zeros	3	2	2	5	4
Cost Per Design	2	3	5	3	5
Cost For Multiple Designs	4	2	5	1	5
Yield	5	3	3	3	4
ASP Scaling	5	3	4	2	4
Capable Frequencies	1 – > 100 GHz	1 – 40 GHz	1 – 40 GHz	0.1 – 40 GHz	DC – 20 GHz
Best-Suited Frequencies	6 GHz – mmWave	5 – 20 GHz	5 – 20 GHz	1 – 20 GHz	DC – 6 GHz
Simulated vs. Measured Accuracy	5	4	3	3	3



▲ Fig. 2 Performance metrics of a microwave filter.



▲ Fig. 3 Sample of 24 typical MMIC filters from a lot of > 8000, showing fabrication repeatability.

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a MMIC filter can be significantly smaller than an equivalent laminate filter. Any system revisions are easier to absorb with a small footprint.

Design flow risk — MMIC filters use a very well-vetted design flow, with first-pass success the standard expectation. The time to a successful design is understood and can be planned with confidence. A laminate design done in-house may or may not meet the schedule.

MMIC VS. THIN FILM

On the surface, a MMIC filter and a thin film filter appear similar: both are surface mountable with standard pick and place machines and reflow ovens. Both offer the ability to test and guarantee performance. Both are smaller than a laminate filter. The advantages of a MMIC filter over thin film are subtle and involve the manufacturing process used to create each type:

Size — While both are small, a MMIC filter can be 10× smaller than an equivalent thin film filter due to the high dielectric constant

of GaAs, the small lines and spaces realized with MMIC lithography and the availability of extremely small, lumped element inductors and capacitors.

Substrate — GaAs has a Dk of 12.9, while alumina (the most common thin film material) has a Dk of 9.8. GaAs also has a superior dielectric loss tangent.

Repeatability — The GaAs substrate material used to fabricate MMICs is a very tightly controlled single crystal produced in high volume. The dielectric constant and thickness are nearly identical from wafer to wafer. MMIC processing tolerances are exceptional—measured in fractions of a micron—owing to the decades of knowledge in the semiconductor manufacturing industry. Thin film circuit fabrication is a boutique technology understood by only a few domestic firms, and their manufacturing processes are not well controlled in comparison to ICs. To illustrate the repeatability of MMIC filters, **Figure 3** shows the variation in the insertion

loss of a sample of filters from a production lot of over 8000 filters.

Scalability — Closely related to repeatability is scalability. Wafers for GaAs can be larger than thin film—they are usually 6 in. for GaAs MMIC versus 2 in. for thin film—and they can be run in larger lots through the factory. For these reasons, MMIC filters can easily and quickly scale to millions of units. By contrast, the thin film industry has consolidated in recent years, partly forced by persistent capacity constraints. Thin film providers often struggle to meet volume needs.

Cost — For a single design, a MMIC is more expensive. For multiple designs—typically four or more—MMIC designs have cost parity with thin film and can even be lower cost. MMIC manufacturing is well suited for multi-project wafers, meaning many designs can be run on the same mask, and once a design is in production, the repeatability and scalability translate to a massive cost advantage. As a rule of thumb, cost savings can be achieved with MMIC filters once volumes exceed hundreds of pieces.

High Frequency Performance — The fine lines and gaps of MMIC lithography and the relatively thin substrates support MMIC filters easily covering frequencies beyond 100 GHz. Thin film filters struggle in performance and consistency above 20 GHz.

Integration — A MMIC filter can be integrated directly with another MMIC function such as an amplifier or switch. It can easily be co-packaged into a standard surface-mount package or multi-chip module.

THE PROMISE OF MMIC FILTERS

Figure 4 shows the performance of four recent MMIC filters developed at Marki, demonstrating the agreement between the simulation and measurement. The simulations are the original design files, with no tuning to match experimental results. The four filters range from four to eight orders and employ different topologies. Owing to the novel capabilities of the MMIC process, some of these filters use lumped elements to enable topologies that

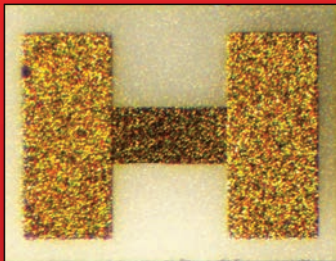
The advertisement features a dark blue background with a subtle circuit board pattern. At the top, the company name 'Quantic™ Wenzel' is displayed in large, white, sans-serif font. Below it, the headline 'Achieve full spectrum dominance with our ultra-low phase noise frequency solutions.' is written in a bold, orange, sans-serif font. To the left of the headline, white text provides details about an event: 'Explore our cutting-edge frequency solutions for electronic warfare applications at the 2022 Association of Old Crows International Symposium & Convention. Washington, D.C. October, 25-27 Booth 100'. On the right side, there are three circular inset images: the top one shows a small, rectangular electronic component; the middle one shows a fighter jet in flight against a cloudy sky; the bottom one shows a person's hands working on a circuit board. At the bottom of the graphic, the website 'quanticwenzel.com' and phone number '[512] 835-2038' are listed in orange text.

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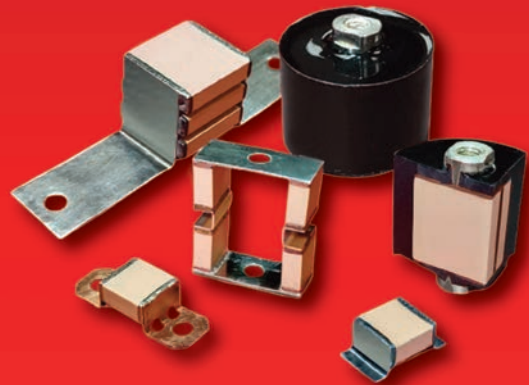
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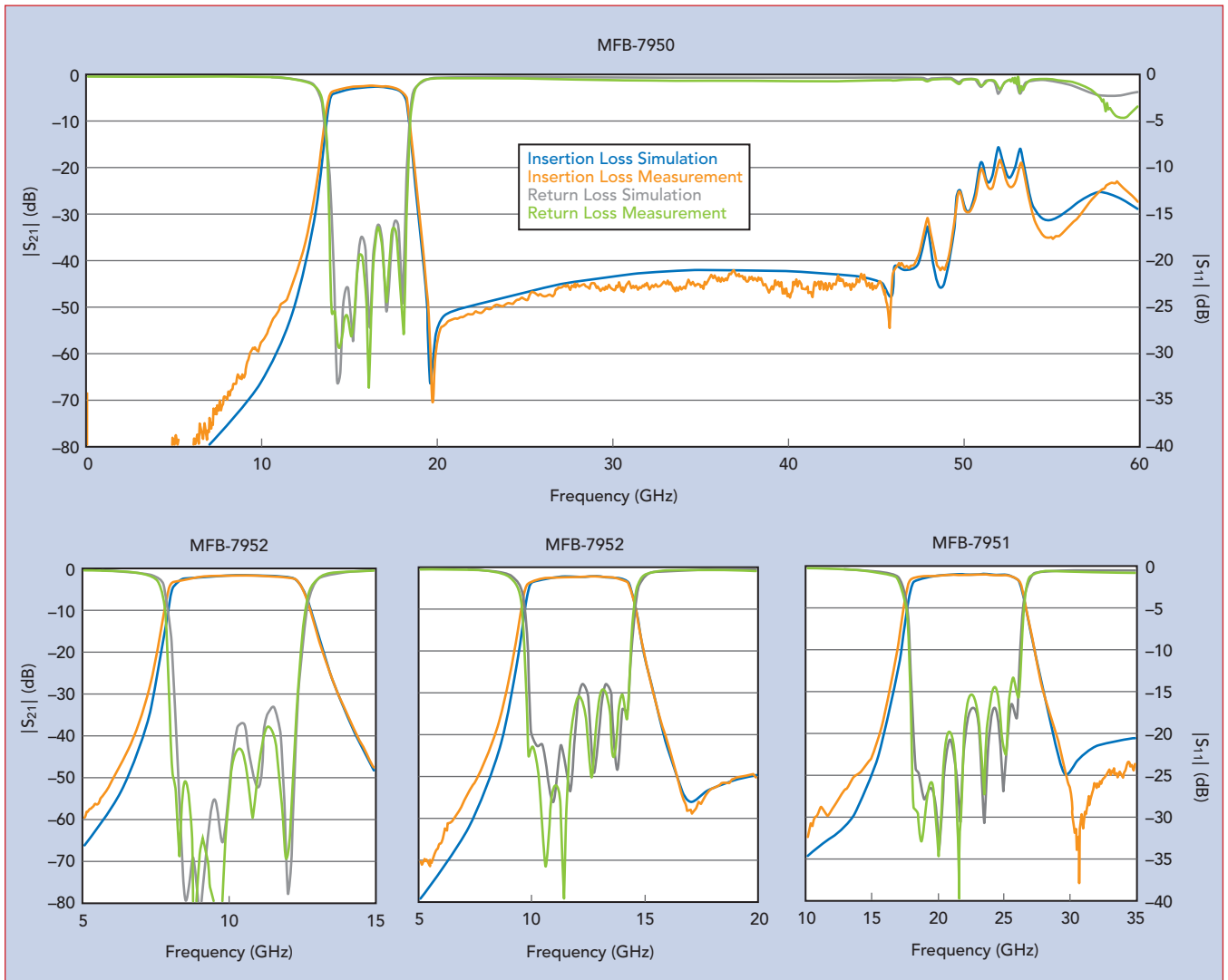


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▲ **Fig. 4** Comparison of simulated and measured responses for four filter designs, each 3.1 mm x 3.1 mm or smaller and fitting in a 5 x 5 QFN package.

cannot be fabricated as thin film or laminate circuits.

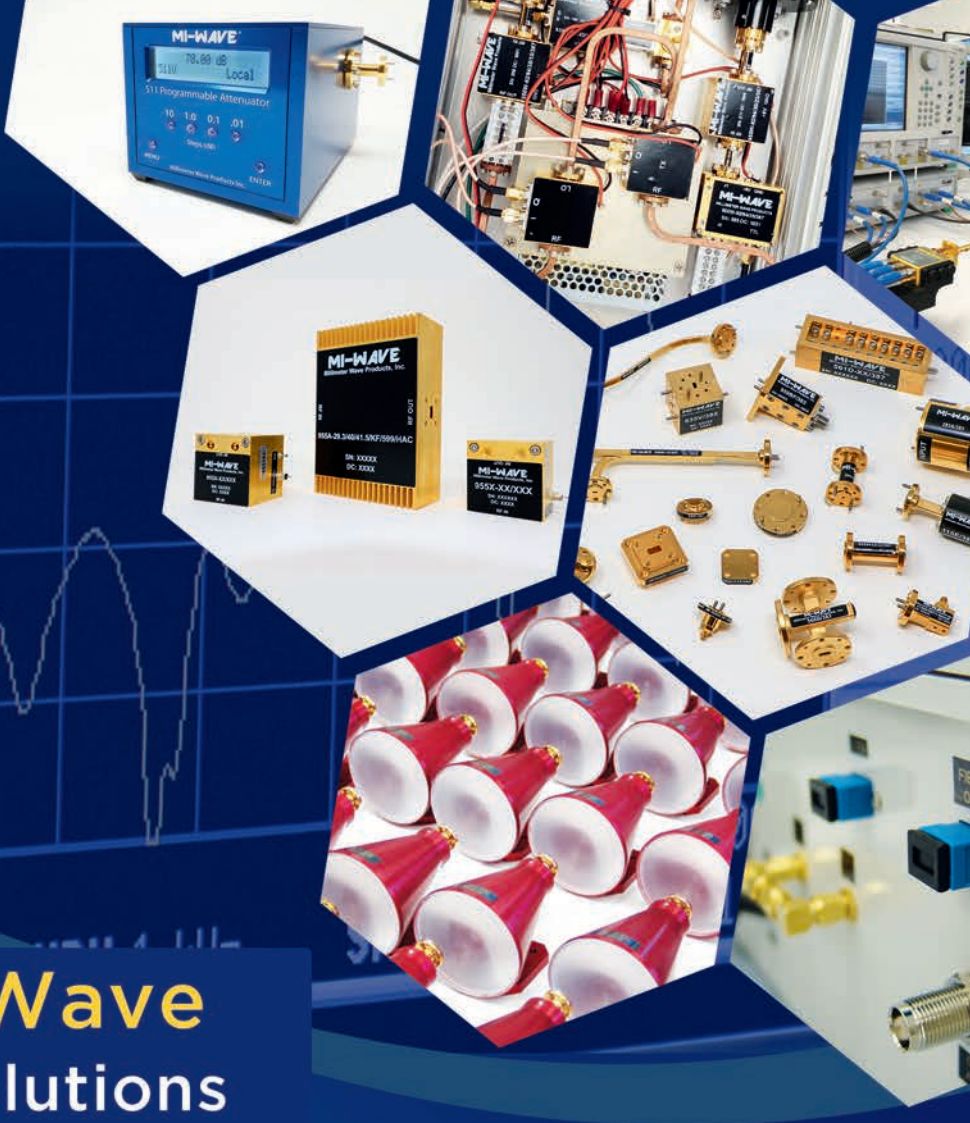
Lumped and quasi-lumped topologies offer several benefits including filter miniaturization and re-entrant mode mitigation. For example, the MFB-7950 response shows the re-entrant mode is well beyond 3fo, a characteristic advantage of the loaded resonator technique. The fine geometric features available with the process enable precise tuning and optimization of features, such as transmission zeros via cross-coupling of resonators.

These results in Figure 4 show near-perfect match between simulation and measurement. This is the most important feature. By developing the design flow and optimization procedure over several years, Marki has shown that it is possible to

quickly and accurately arrive at a design that will be reproduced by the foundry. First-pass design success means the development cycle is as short as possible: New designs can be turned in days, followed by fabrication and packaging lead times of 10 to 14 weeks, on average. This puts the MMIC development cycle in line with traditional manufacturers, albeit with significantly better first-pass confidence that “you measure what you simulate.”

Historically, semiconductor technology was not considered viable for a high mix of highly customized filters manufactured in low volume. It was widely assumed that the upfront costs of MMIC development negated the lower per-unit cost in production. We have discovered that a well-crafted MMIC design

flow achieves first-pass success and the approach is cost-effective for custom filters, as long as the upfront costs are shared across multiple designs. Trends toward smaller form factor, higher volume, higher frequency filter requirements provide further incentive for custom MMIC filter solutions. MMIC filter technology offers a lower risk path to first-pass design success compared to incumbent technologies. Marki has demonstrated competitive filter performance at a fraction of the size of competing technologies, with improvements in performance and size ongoing. Enabled by advanced design and process improvements, the dream of best-in-class, rapidly designed, small form factor MMIC filters has become a reality. ■



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Low Noise Tuning Diodes for Voltage-Controlled Oscillators

Ulrich L. Rohde

Synergy Microwave, Paterson, N.J., Center for Integrated Sensor Systems, Universität der Bundeswehr, Munich, Germany

Ignatz Eisele

Center for Integrated Sensor Systems, Universität der Bundeswehr, Munich, Germany, Fraunhofer EMFT, Munich, Germany

Leonhard Sturm-Rogon, Robert Wieland and Wilfried Lerch

Fraunhofer EMFT, Munich, Germany

An oscillator noise model distinguishes between various noise sources and predicts their influence on voltage-controlled oscillator (VCO) single sideband noise. Tuning diodes are the most critical elements. A test oscillator validates the predicted performance. An equivalent noisy resistor is introduced as a figure of merit for low noise diodes. Finally, the important fabrication considerations for low noise diodes are presented and validated in the test oscillator. At 10 kHz offset, the noise contribution of optimized tuning diodes in the oscillator adds only 10 dB of noise compared to a fixed capacitor design.

Nearly all RF oscillators are voltage-controlled. The main single sideband noise contribution comes from the transistor's intrinsic noise sources and the noise contribution of the tuning diode. The published flicker noise exponent (AF) and flicker noise coefficient (KF) values for transistors are usually determined at μV RF levels and normal DC operating conditions. As the RF level in an oscillator is much greater, this must be considered in the circuit analysis.

Most semiconductor companies changed their production processes for tuning diodes due to requirements of digital applications with the result that oscillator phase noise deteriorated. Also, none of the diode manufacturers specifies phase noise in oscillators, as there are too many variations of oscillator circuits available.

To develop and characterize low noise tuning diodes, it is necessary to describe the appropriate oscillator, analyze its critical semiconductor components and finally compare the tuning diode with the ideal case of

a fixed capacitor. This article follows that guideline to verify the quality of newly developed tuning diodes.

ANALYSIS OF THREE-REACTANCE OSCILLATORS

A generalized circuit for an oscillator is shown in **Figure 1**. This is typically referred to as a Colpitts oscillator.¹ It has a capacitive voltage divider, Z_1 and Z_2 , and an inductor Z_3 . Its phase noise can be determined with a microwave simulator. With these programs, however, it is not possible to distinguish the individual noise contributions to the output signal. Therefore, a direct analysis of the oscillator circuit equations is presented here. The active device is a three-terminal device, typically a transistor.²

Figure 2 shows the Colpitts oscillator including leads and package parasitics. In practice, the lossy part of a tuned circuit is the inductor. R_{s1} is the resonator loss. Splitting the input impedance Z_{IN} (see **Figure 1**) of the Colpitts oscillator into real and imaginary parts we obtain:

$$R_{NEQ} = \frac{R_N}{(1 + \omega^2 Y_{21}^2 L_p^2)} \quad (1a)$$

$$\frac{1}{C_{EQ}} = \left\{ \frac{1}{(C_1 + C_p)C_2} - \left[\frac{\omega^2 Y_{21} L_p}{(1 + \omega^2 Y_{21}^2 L_p^2)} \right] \left[\frac{Y_{21}}{\omega(C_1 + C_p)C_2} \right] \right\} \quad (1b)$$

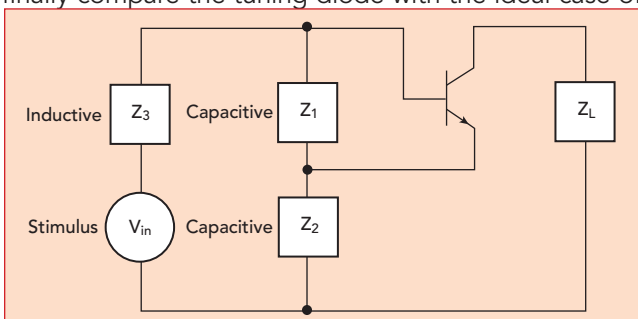


Fig. 1 Generalized oscillator circuit using an amplifier model. Z_L is the load.



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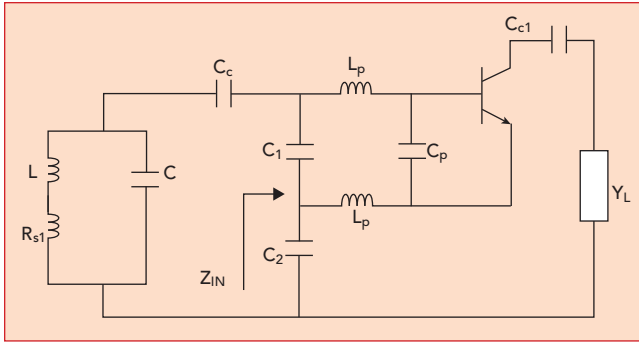


Fig. 2 Colpitts oscillator with base lead inductances, L_p , and package capacitance C_p .^{3, p. 132}

Where:

R_N : Negative resistance without lead inductance and package capacitance

R_{NEQ} : Negative resistance with base-lead inductance and package capacitance

C_{EQ} : Equivalent capacitance with base-lead inductance and package capacitance.

The method shown is based on one-port oscillator design.^{3,4,5} The negative real part of Z_{IN} compensates the resistor loss of the parallel tuned circuit.

Equation (1b) can be solved for C_{EQ} , see equation (2a), imaginary part. The exact calculation of the "noisy" negative real part of the resistance $Z_{IN, package}$, which is needed to compensate the tuned circuit loss, is given by:

$$Z_{in | package} = - \left[\frac{Y_{21}}{\omega^2 (C_1 + C_p) C_2} \frac{1}{(1 + \omega^2 Y_{21}^2 L_p^2)} \right] - j \left[\frac{(C_1 + C_p + C_2)}{\omega (C_1 + C_p) C_2} - \frac{\omega Y_{21} L_p}{(1 + \omega^2 Y_{21}^2 L_p^2)} \frac{Y_{21}}{\omega (C_1 + C_p) C_2} \right] \quad (2a)$$

The left part is the negative part of the "noisy" input resistance. The intrinsic value R_N is:

$$R_N = - \frac{Y_{21}}{\omega^2 C_1 C_2} \quad (2b)$$

This is a noisy electronically generated negative resistance. It combines all internal noise sources to be modulated on the oscillator carrier frequency.

Leeson's Empirical Phase Noise Model

E.J. Baghdady et al.⁶ first gave the definition of phase noise. Single sideband phase noise equation (3) is based on David Leeson,⁷ Scherer and Rohde.⁸ Scherer was the first to introduce the flicker effect to the Leeson equation and Rohde the first to add the AM-to-PM (VCO, last term in the equation) conversion effect, caused by the nonlinear capacitance of the active devices.

Leeson's complete phase noise equation is given by:

$$\mathcal{L}(f_m) = 10 \log \left\{ \left[1 + \frac{f_0^2}{(2f_m Q_L)^2} \right] \left(1 + \frac{f_c}{f_m} \right) \frac{FkT}{2P_{sav}} + \frac{2kTRK_0^2}{f_m^2} \right\} \quad (3)$$

Where:

$\mathcal{L}(f_m)$ = ratio of sideband power in 1 Hz bandwidth at f_m to total power in dB

f_m = frequency offset, or modulating frequency

f_0 = center frequency

f_c = flicker corner frequency

Q_L = loaded Q of the tuned circuit, should be half of the unloaded resonator Q_0 (Matching for Power)

F = large signal noise factor

$kT = 4.1 \times 10^{-21}$ at 300 [K] (room temperature)

P_{sav} = average power at oscillator output

R = equivalent noise resistance of tuning diode (typically 200 [Ω] to 10 [k Ω])

K_0 = oscillator voltage gain

k = Boltzmann constant.

Equation (3) is shown graphically in **Figure 3**. The problem is that necessary data, like output power, large signal noise figure, loaded Q and flicker noise are not known a priori. The other problem is that it does not provide the actual noise contribution of the semiconductor devices. It is shown below that the phase noise contribution of the tuning diode in VCOs is the critical part, and not the transistor itself. The fixed frequency oscillator is the best phase noise case.

Depending on the relation between f_c and $f_0/2Q_L$, there are two cases of interest. For the low-Q case the spectral phase noise is unaffected by the Q of the resonator, but the $\mathcal{L}(f_m)$ spectral density will show a $1/f^3$ and $1/f^2$ dependence close to the carrier. For the high Q case, a region of $1/f^3$ and $1/f$ should be observed near the carrier.

At small offset frequencies from the carrier, the phase noise exhibits a slope of $1/\Delta f^3$, i.e. 30 dB per decade. This

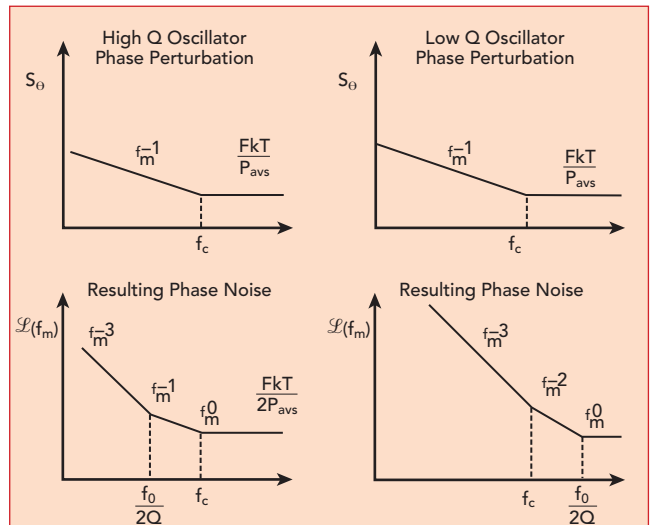


Fig. 3 Equivalent feedback models of oscillator phase noise.^{3,8}

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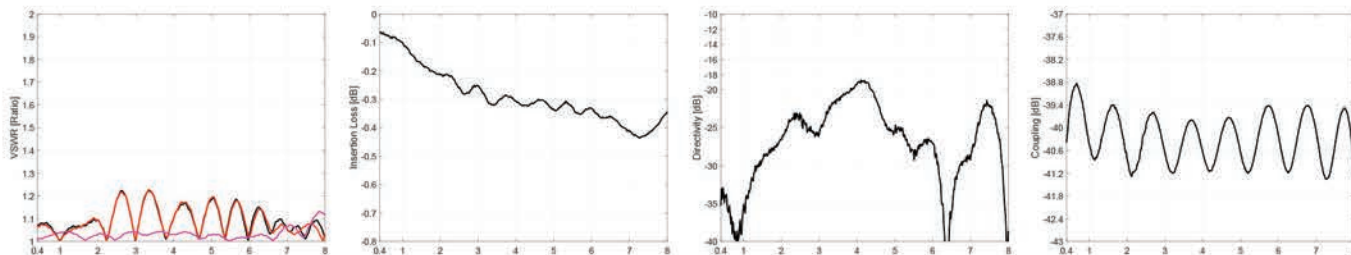


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				Max.(:1)			Max.(dB)		Min.(dB)
0.4~8	D3002H004080	120	30	1.3	1.3	0.8	30±1.0	±0.8	18
	D4002H004080	120	40	1.3	1.3	0.8	40±1.0	±0.8	18
	D3005H004080	250	30	1.4	1.4	0.6	30±0.9	±1.3	14
	D4005H004080	250	40	1.4	1.4	0.6	40±1.0	±1.4	14
	D3008H004080	400	30	1.4	1.4	0.6	30±0.9	±1.3	14
	D4008H004080	400	40	1.4	1.4	0.6	40±1.0	±1.4	14
	D3012H004080	600	30	1.4	1.4	0.6	30±0.9	±1.3	14
	D4012H004080	600	40	1.4	1.4	0.6	40±1.0	±1.4	14

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TABLE 1

f_c vs. I_C

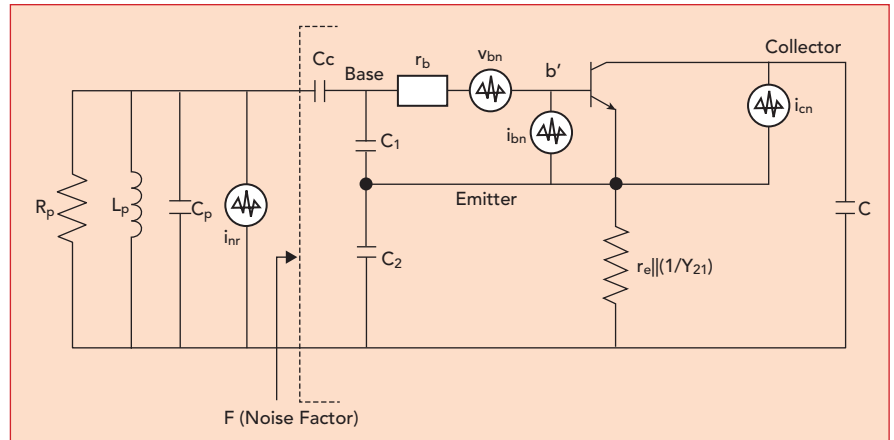
I_C (mA)	f_c (kHz)
0.25	1
0.5	2.74
1	4.3
2	6.27
5	9.3

(Source: Motorola)

region is dominated by flicker noise up-conversion. Particularly, in CMOS this is a challenge, since the $1/f$ -noise corner frequency is very high. Above that, the slope is 20 dB per decade. This is the offset frequency region dominated by thermal noise up-conversion. Finally, at higher offset frequencies from the carrier the spectrum is flat, limited by the noise floor of the active circuit (see Figure 2), given by kT/P_{sig} .⁹ For very high Q resonators, the flicker corner frequency f_c moves to higher frequencies, independent of the transistor (filter effect).

Table 1 shows f_c as a function of the collector current I_C for a typical small-signal microwave bipolar junction transistor (BJT). $I_{C(max)}$ of this transistor is about 10 mA. The corner frequency increases non-linearly with current (DC).

Note that f_c , which is defined by AF and KF in the SPICE model, increases significantly with I_C . This gives a clue about how f_c changes when a transistor oscillates at differ-



▲ Fig. 4 Colpitts oscillator circuit configuration.

ent current levels. Because of the bias-point shift that occurs during oscillation, an oscillating BJT's average I_C is higher than its small-signal I_C . KF is therefore higher for a given BJT operating as an oscillator than for the same transistor operating as a small-signal amplifier. Generally, f_c varies with device type as follows: Si JFETs, 50 Hz and higher; microwave RF BJTs, 1 to 10 kHz (as above); MOSFETs, 10 to 100 kHz and GaAs FETs, 10 to 100 MHz.

Several observations can readily be made. One obvious way to reduce phase noise is to increase the power or oscillation amplitude. This, however, is limited in practical oscillators due to the supply level. Another, more practical, possibility is to increase the quality factor of the tank. The first part of equation (1), describ-

ing $1/\Delta\omega^2$, corresponds to the thermal noise part of the spectrum. Multiplying by another $1/\Delta\omega$ describes the flicker noise part of the phase noise spectrum. Flicker noise is described empirically, and no insight is provided into the flicker noise up-conversion mechanisms; however, it can still be concluded that increasing the voltage swing or increasing the quality factor of the tank will reduce flicker noise in this region.

Equation (4),⁹ based on Leeson's equivalent circuit and the special case of the Colpitts oscillator, yields exact values for P_{sav} , Q_L and F that are needed to solve Leeson's equation. The approach shown here is novel. We can now calculate the output power. The factor of 1000 is needed since the result is expressed in dBm and a function of n and C_1 .

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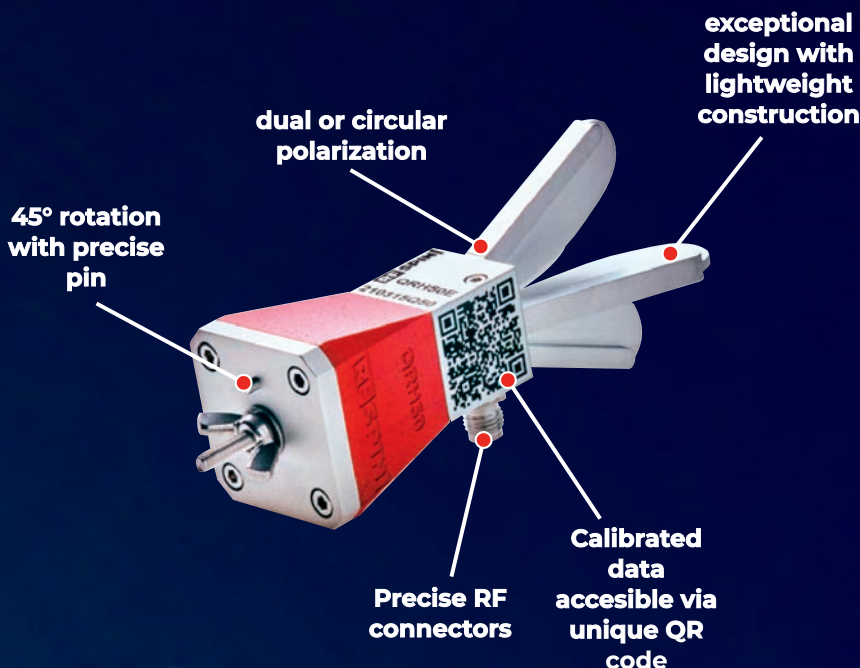
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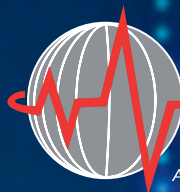
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$$[P_0(n, C_1)]_{\text{dBm}} = 10 \log \left\{ \left[\frac{(V_{ce} = -0.7)^2}{4(\omega_0 L)^2} \right] \left[\frac{Q_L^2 \left[C_1^2 \left(\frac{C_1}{n-1} \right)^2 \omega_0^4 L^2 \right]}{Q_L^2 \left(C_1 + \frac{C_1}{n-1} \right)^2 + \omega_0^4 L^2 C_1^2 \left(\frac{C_1}{n-1} \right)^2} \right] R_L * 1000 \right\} \quad (4)$$

Where 0.7 V is the high current saturation voltage and V_{ce} is the collector emitter voltage $< V_{cc}$.

To calculate the loaded Q (Q_L) consider the unloaded Q (Q_0) and the loading effect of the transistor. There we consider the influence of the large signal condition Y_{21}^* . The inverse of this is responsible for the loading and reduction of Q_L .

$$Q^* = \frac{\omega_0 \times \left| \frac{1}{Y_{21}^*} \right| (C_1 + C_2)}{1 - \omega_0^2 C_1 L (Q = Q_0)}; \quad (5)$$

$$\text{and finally } Q_L = \frac{Q_0 \times Q^*}{Q_0 + Q^*}$$

The transistor noise factor can also be calculated under large signal conditions. Considering Y_{21}^* , this noise calculation is based on general noise calculations

such as those of Pucel and Rohde.¹⁰ An equivalent procedure can be found for FETs as well.

Oscillator Noise Factor

Figure 4 shows the oscillator equivalent circuit configuration for the purpose of analyzing F with respect to the oscillator feedback components (C_1 and C_2), which are needed to predict F in Leeson's Equation. The objective is to determine the oscillator circuit parameters that influence F, thereby influencing oscillator phase noise.

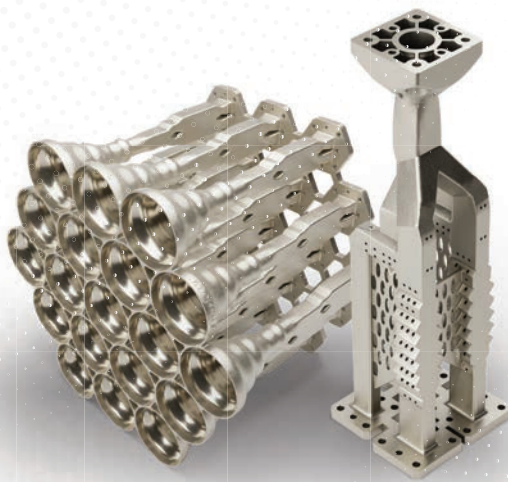
F for the transistor in Figure 4 is:

$$F = 1 + \frac{Y_{21}^* C_2 C_C}{(C_1 + C_2) C_1} \left[\gamma_b + \frac{1}{2\gamma_e} \left(\gamma_b + \frac{(C_1 + C_2) C_1}{Y_{21}^* C_2 C_C} \right)^2 \left(\frac{1}{\beta} + \frac{f^2}{f_T^2} \right) + \frac{\gamma_e}{2} \right] \quad (6)$$

For fixed capacitors C_1 , C_2 , the following components contribute to oscillator noise:

- Thermal noise associated with the loss resistance of the resonator
- Thermal noise associated with the base resistance of the transistor
- Shot noise associated with the base bias current

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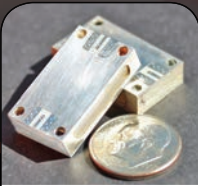
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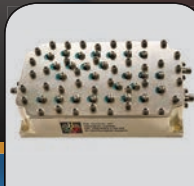
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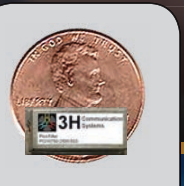
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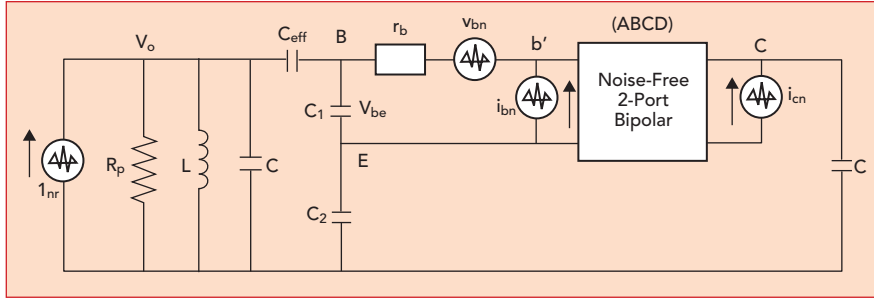


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▲ Fig. 5 Oscillator calculation using the ABCD matrix.³, p. 132

- Shot noise associated with the collector bias current. An oscillator circuit with the contribution of all four noise sources is shown in **Figure 5**.

Using an oscillator circuit with a noisy resonator, the total noise of the oscillator in Figure 5 can be determined.³ Consider the effective capacitance C_{eff} :

$$C_{eff} = C + \frac{C_1 C_2}{C_1 + C_2} \quad (7)$$

The phase noise contribution (PN) from the oscillator circuit with a 2-port [ABCD] matrix is:

$$PN_{inr}(\omega_0 + \Delta\omega) = \frac{4KT}{R_p} [NFT_{inr}(\omega_0)]^2 = \frac{4KT}{R_p} \left\{ \frac{1}{2} \left[\frac{1}{2\omega_0 C_{eff}} \right] \left[\frac{\omega_0}{\Delta\omega} \right] \right\}^2 \quad (8a)$$

= the phase noise contribution from the resonator tank.

$$PN_{Vbn}(\omega_0 + \Delta\omega) = 4KT r_b [NFT_{Vbn}(\omega_0)]^2 = 4KT r_b \left\{ \frac{1}{2} \left[\frac{C_1 + C_2}{C_2} \right] \left[\frac{1}{2Q} \right] \left[\frac{\omega_0}{\Delta\omega} \right] \right\}^2 \quad (8b)$$

= the phase noise contribution from the base spreading resistance.

$$PN_{ibn}(\omega_0 + \Delta\omega) = 2qI_b [NFT_{ibn}(\omega_0)]^2 = 2qI_b \left\{ \frac{1}{2} \left[\frac{C_2}{C_1 + C_2} \right] \left[\frac{1}{\omega_0 Q C_{eff}} \right] \left[\frac{\omega_0}{\Delta\omega} \right] \right\}^2 \quad (8c)$$

= the phase noise contribution from the base current.

$$PN_{ifn}(\omega_0 + \Delta\omega) = \frac{K_f I_b^{AF}}{f_m} [NFT_{ifn}(\omega_0)]^2 = \frac{K_f I_b^{AF}}{f_m} \left\{ \frac{1}{2} \left[\frac{C_2}{C_1 + C_2} \right] \left[\frac{1}{2\omega_0 Q C_{eff}} \right] \left[\frac{\omega_0}{\Delta\omega} \right] \right\}^2 \quad (8d)$$

= the phase noise contribution from the flicker noise of the transistor.

$$PN_{icn}(\omega_0 + \Delta\omega) = 2qI_c [NFT_{icn}(\omega_0)]^2 = 2qI_c \left\{ \frac{1}{2} \left[\frac{C_2}{C_1 + C_2} \right] \left[\frac{1}{2\omega_0 Q C_{eff}} \right] \left[\frac{\omega_0}{\Delta\omega} \right] \right\}^2 \quad (8e)$$

= the phase noise contribution from the collector current.

AM-to-PM Conversion

The transition from a basic oscillator to a VCO is achieved by replacing all or a part of the resonator capacitor with a voltage dependent variable capacitor, typically a tuning diode or varactor.² The RF voltage across the depletion capacitance modulates the operating frequency. FM and PM cannot be distinguished at a constant f_m ;

however, with a change in f_m , the FM modulation index will change and the PM modulation index will not.

To calculate the total phase noise, an equivalent noise resistance R_{eq} of the tuning diode is defined. When inserted in Nyquist's equation it results in a frequency offset dependent noise voltage V_n across the tuning diode:

$$V_n = \sqrt{4kTR_{eq}\Delta f} \quad (9)$$

where $kT = 4.2 \times 10^{-21}$ at 300 K, and Δf is the offset from the carrier.

This noise voltage generated from the tuning diode is now multiplied with the VCO gain K_o , resulting in an rms frequency deviation Δf_{rms} . This can be translated into an equivalent peak phase deviation θ_d :

$$\theta_d = \frac{K_o \sqrt{2}}{\Delta f} \times V_n \text{ rad in a 1 Hz bandwidth} \quad (10)$$

This is converted into the single sideband (SSB) signal-to-noise ratio expressed in dB

$$SSB \text{ S/N} = 20 \times \log(\theta_d / 2) \text{ dB} \quad (11)$$

Comparing the SSB noise of the oscillator with a fixed capacitor and an identical capacitance value of the tuning diode determines the equivalent noise resistor R_{eq} . The lower the resistor the better the quality of the diode. All relevant information is provided by Rohde and Rudolph.⁹

DIODE FABRICATION AND SINGLE DEVICE PERFORMANCE

A Si tuning diode consists of a p-n junction. Contacting an n-doped and a p-doped region, the mobile charge carriers (electrons and holes) are pulled away from the junction and a depletion zone is created that acts as a capacitor. By applying a reverse bias voltage (V) the depletion zone width x_D increases. For the n-type region it is given by:

$$x_D = \sqrt{\frac{2\epsilon_0 \epsilon_{Si}}{eN_D(X)}} (V_D + V) \quad (12)$$

$\epsilon_0 \epsilon_{Si}$ is the dielectric constant of Si, e is the elementary charge and $N_D(x)$ is the donor concentration. The diffusion voltage V_D is given by:

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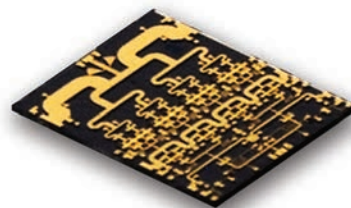
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$$V_D = \frac{W_C - W_F}{e} \quad (13)$$

where W_C is the energy of the conduction band edge and W_F is the Fermi energy.

For the p-type region, the donor concentration is replaced by the acceptor concentration.

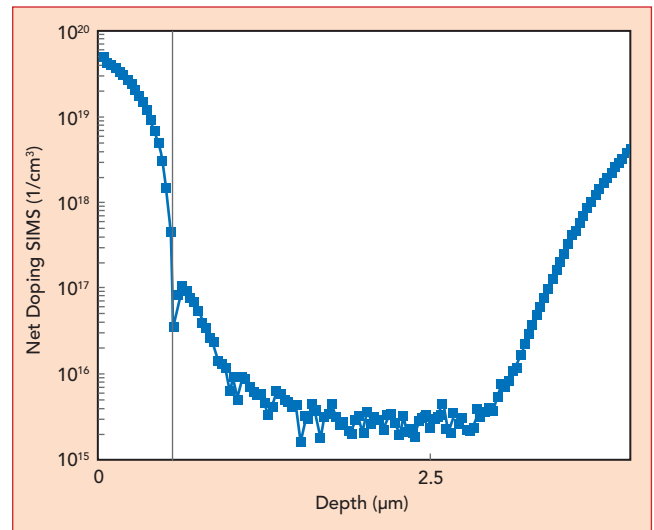
The voltage dependent capacity $C(V)$ can be written as:

$$C(V) = \frac{A\epsilon_0\epsilon_{Si}}{X_D} = C_0 / \left(1 + \frac{V}{\phi}\right)^\gamma \quad (14)$$

where $\gamma = 0.5$ characterizes the theoretical value for an abrupt junction diode with constant doping concentration in the depletion zone.

For a VCO, several more parameters must be considered, such as frequency range, linearity, series resistance and noise level. So-called hyperabrupt tuning diodes¹¹ are widely used for VCOs and this article presents results regarding these requirements. Using epitaxy, ion implantation and careful thermal management, high-quality hyperabrupt diodes are realized with extremely low noise levels.

Highly doped n-type 200 mm Si wafers with (100) orientation are used to achieve low series resistance. In a first step, an n-type epitaxial layer with a thickness of several micrometers and a doping concentration in the



▲ Fig. 6 SIMS profile of the hyperabrupt tuning diode.

range of 1×10^{15} to $1 \times 10^{16} \text{ cm}^{-3}$ is grown. The p⁺-region is fabricated by ion implantation.

A SIMS profile of the total stack after annealing is shown in **Figure 6**. In principle it is possible to create even sharper doping transitions,¹² however, these techniques (e.g. molecular beam epitaxy) are not suited for mass production. To avoid lateral spreading of the electric field, a guard ring structure is integrated. Diodes with an active area of $A = 0.118 \text{ mm}^2$ as well as $A = 0.037 \text{ mm}^2$ are fabricated on the same wafer.

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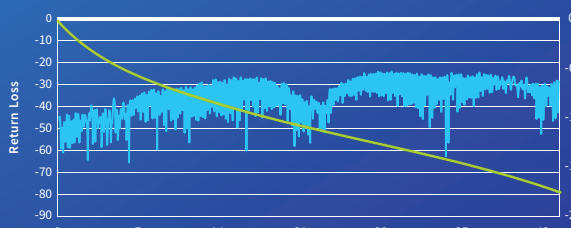


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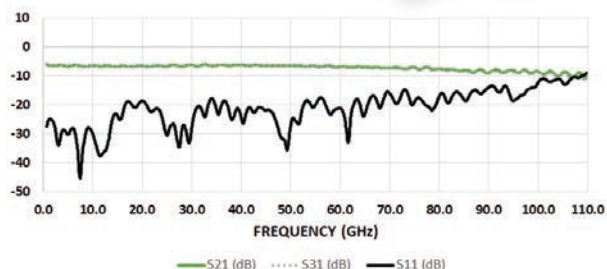
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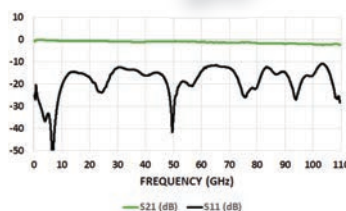
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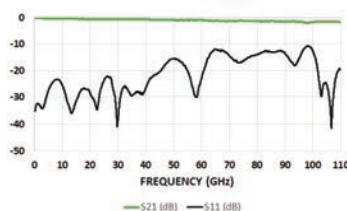
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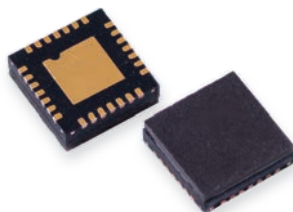


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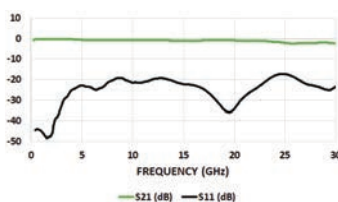
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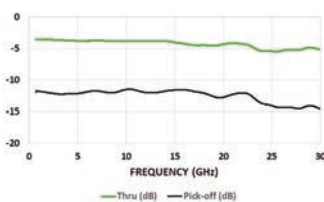
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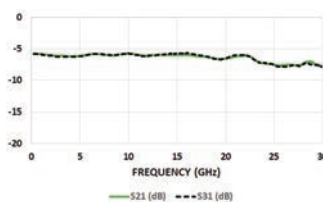
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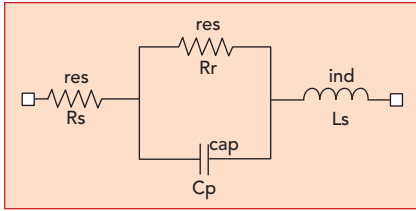
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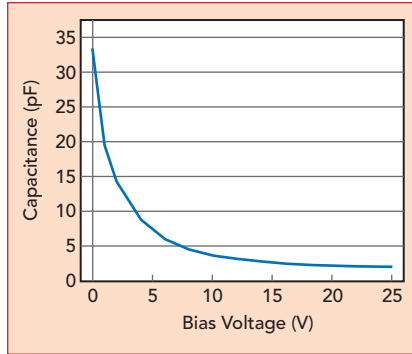


▲ Fig. 7 Diode equivalent circuit.

For the front-side metallization a Ti/TiN barrier is sputtered followed by Al/1%Si. For the backside a gold-based metallization is chosen to enable soldering in the package.

The noise of the hyperabrupt diodes—and therefore the resonator noise—depends on the quality factor $\text{Im}(Z)/\text{Re}(Z)$. The higher the quality factor of the resonator, the lower the oscillator noise. Considering the equivalent circuit of the diode (see Figure 7), one must consider two parameters:

1) The crystalline quality of the Si in the depletion zone should be as high as possible to avoid any point defects such as vacancies or interstitials, which act as scattering centers and increase the noise level.¹³ As a consequence, the resistance R_r for



▲ Fig. 8 Capacitance tuning range vs. reverse bias on the $A = 0.118 \text{ mm}^2$ diode measured at 500 MHz.

reverse bias must be as high as possible. This can be achieved by careful annealing steps.

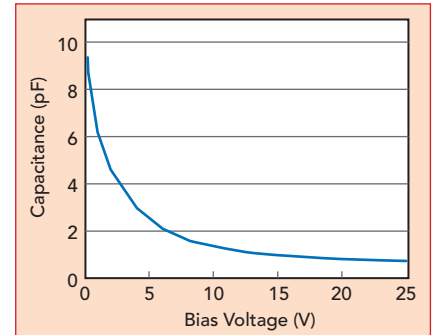
2) The real part of the impedance, which mainly consists of the contact series resistances and the wiring of the package, must be minimized. For this purpose, the wafers are thinned to $120 \mu\text{m}$. The resulting series resistance R_s of the bare die, measured at 5 GHz and 2 V reverse bias voltage, amounts to 0.8Ω for the larger diode and 1.3Ω for the smaller diode.

Wafer Level Measurements

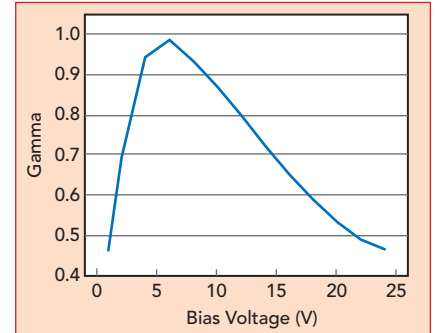
The breakdown voltage for both types of diodes is 31 V. For the larger diodes, wafer level measurements of capacitance (measured at 500 MHz) as a function of reverse bias voltage is shown in Figure 8. A capacitance $C_1 = 19 \text{ pF}$ is measured at a reverse bias of 1 V and $C_{25} = 2 \text{ pF}$ at 25 V. The resulting capacitance ratio C_1/C_{25} is 9.5.

For the smaller diodes, capacitance versus voltage behavior is shown in Figure 9. A capacitance $C_1 = 6.2 \text{ pF}$ is measured at a reverse bias of 1 V and $C_{25} = 0.75 \text{ pF}$ at 25 V. The resulting capacitance ratio C_1/C_{25} is 8.3.

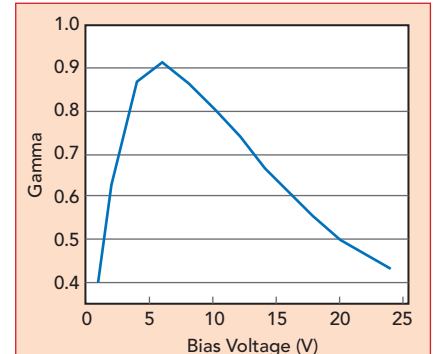
In contrast to the above derived simple depletion approximation,



▲ Fig. 9 Capacitance tuning range vs. reverse bias on the $A = 0.037 \text{ mm}^2$ diode measured at 500 MHz.



▲ Fig. 10 γ vs. bias voltage for the $A = 0.118 \text{ mm}^2$ diode measured at 500 MHz.



▲ Fig. 11 γ vs. bias voltage for the $A = 0.037 \text{ mm}^2$ diode measured at 500 MHz.

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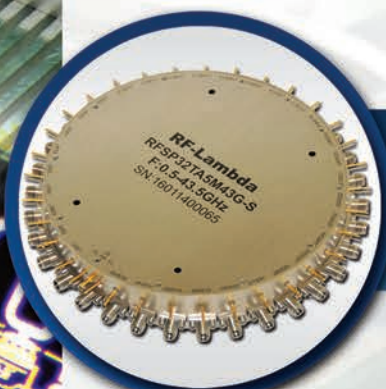


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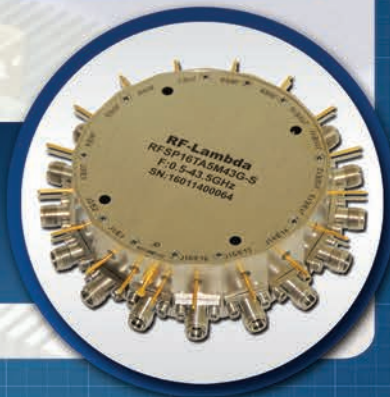


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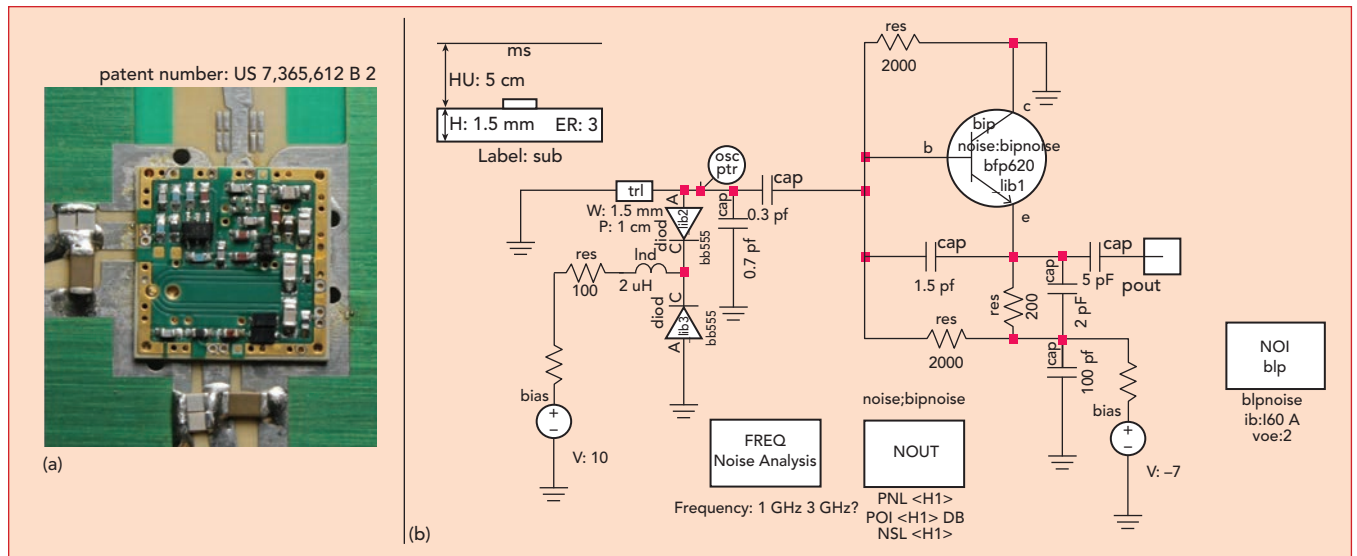


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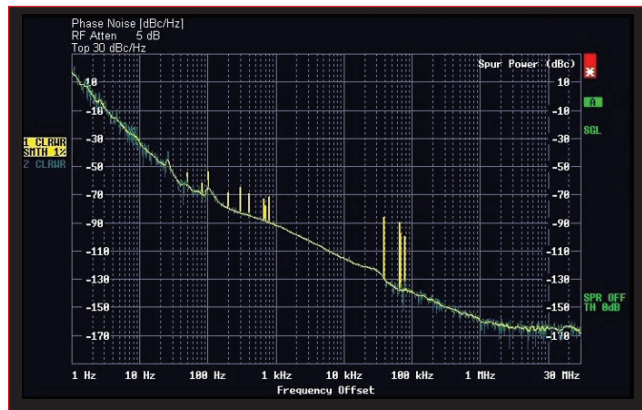
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▲ Fig. 12 1.3 GHz test oscillator with tuning diodes (a) and schematic (b).



▲ Fig. 13 Measured phase noise of the oscillator with a fixed capacitor.

the γ -value of hyperabrupt tuning diodes is no longer constant with reverse bias, however, this value is important for the design of oscillators. Therefore, wafer level measurements are made for the two types of diodes (see **Figures 10** and **11**).

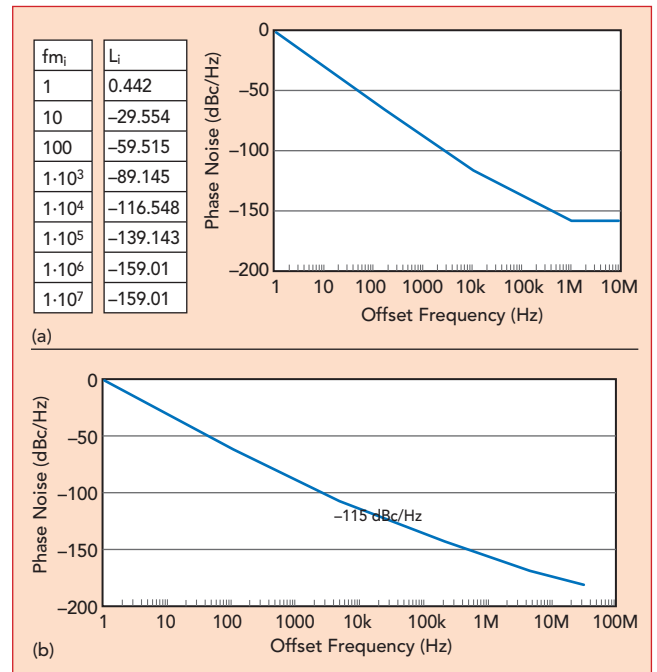
Packaging

After wafer level measurements the wafers are diced and packaged in a QFN type housing with SC79 soldering pads. The front-side contact, which acts as anode, is gold wire bonded, whereas the backside contact, which acts as cathode, is connected to the ground plate. The lead frame is copper.

SIMULATION AND MEASUREMENT OF PHASE NOISE IN A TEST OSCILLATOR

Noise performance of diodes can only be characterized in a test oscillator. It should be noted that different results are obtained for different oscillator designs. The quality of the diodes is demonstrated with the Infineon transistor BFP 620 in an oscillator at 1.3 GHz (see **Figure 12**).

Instead of the tuning diodes, we start with a fixed capacitor of 15.3 pF in parallel with the 0.7 pF capacitor to ground (see **Figure 12b**), for a frequency of about 1.3 GHz. This is the ideal case and acts as a reference.



▲ Fig. 14 Oscillator phase noise without a tuning diode calculated using Leeson's equation (a) and simulated using the Serenade HB microwave simulator (b).

The measured phase noise of this circuit as a function of frequency offset from the center frequency is shown in **Figure 13**. At an offset of 10 kHz it is about -115 dBc/Hz. An offset frequency of 10 KHz is used as this is the closest to the carrier selected in a PLL to compensate microphonic effect and outside the PLL loop frequency where the inherent phase noise dominates. The prediction from the presented model as well as the SPICE data-based simulation (see **Figure 14**) agrees well with the measurement.

Next, the capacitor is replaced by a tuning diode to realize a VCO. According to **Figure 8**, a reverse bias of about 2 V is needed to obtain a comparable capacitance of 15 pF. The resulting measured phase noise plot of the oscillator is shown in **Figure 15**. The phase noise at a 10



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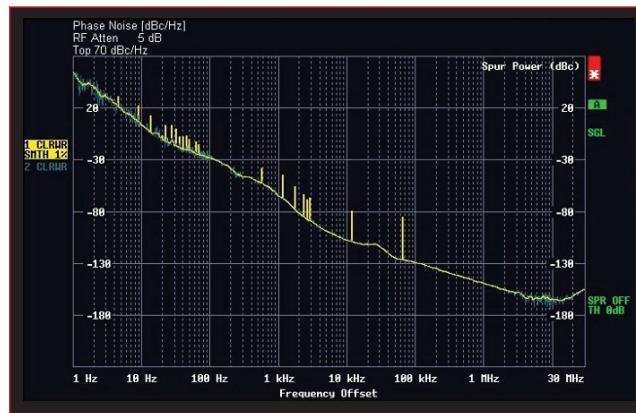


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▲ Fig. 15 Measured phase noise of the oscillator with tuning diodes.

kHz offset is about -107 dBc/Hz, only 8 dB above the level with a fixed capacitor, for an oscillator with a 2 to 1 tuning range. To our knowledge, this is the best value achieved to date.

Equations 9 and 10 are used to perform a backward calculation for the equivalent noise resistor.

For $L(f_m) = -107.41$ dBc/Hz, assuming a K_0 of 120 MHz/V, $\Delta f_{rms} = 0.06$ in a 1 Hz bandwidth.

$$\theta_d = \frac{K_o \sqrt{2}}{f_m} \times V_n = \frac{120 \times 10^6 \sqrt{2}}{f_m} \times 5.02 \times 10^{-10} = 8.519 \times 10^{-6} \text{ rad in 1 Hz bandwidth} \quad (15)$$

For an offset frequency

$$f_m = 10 \text{ kHz } \theta_d = 8.519 \times 10^{-6} / f_m$$

$$\theta_d = \frac{K_o \sqrt{2}}{f_m} \times V_n = \frac{8.519 \times 10^{-6}}{10,000} = \text{rad 1 Hz bandwidth} \quad (16)$$

$$\begin{aligned} \text{Log}(\theta_d / 2) &= \text{log}(4.26\text{E} - 6) = -5.37; \\ L &= 20 \times \text{log}(\theta_d / 2) = -107 \text{ dBc / Hz, QED} \end{aligned} \quad (17)$$

The resulting voltage value $V_n = 5.02 \times 10^{-10} \text{ V}/\sqrt{\text{Hz}}$. Finally, the newly developed diodes have a very low equivalent noise resistance of only 15 Ω .

CONCLUSION

The described noise model for VCOs proves that tuning diodes dominate the sideband noise of oscillators. As a figure of merit for the diodes, an equivalent noise resistor is introduced that describes

the noise spectrum deviation from an ideal case with a fixed capacitor. The newly developed diodes with the same AC characteristics as commercial diodes demonstrate phase noise levels only 8 dB above the value for a fixed capacitor when measured with the same test oscillator. ■

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The Great Debate: Should COTS Components Be Used in Space?

Peter Matthews

Knowles Precision Devices, Cazenovia, N.Y.

The adoption of commercial-off-the-shelf (COTS) parts is a big shift for NASA, since this organization has followed an extensive parts qualification and screening process using MIL-SPECS for decades. Seeking to remain competitive and to provide guidance for missions that are budget constrained, NASA commissioned a NASA Engineering and Safety Center (NESC) study to evaluate the use of COTS parts. The goal of this extensive study was to establish a consistent set of requirements at the agency level to control risk and minimize the impact of part selection and usage on reliability in NASA spaceflight hardware. This article examines some of the industry trends that drove NASA to perform this study, as well as some of the information and recommendations from NASA provided in Phase 1 of this study, which was released in December 2020.¹

When designing a traditional geostationary (GEO) satellite, reliable lifetime operation is crucial. This is because these satellites are typically multi-mission communication platforms that can cost more than \$1 billion to develop, leaving no room for a failure of even the tiniest passive component. These satellites also orbit Earth from 22,300 miles away, so making repairs in the event of a failure is not an option. Therefore, every component used in a GEO satellite has historically been put through a rigorous, and costly, space qualification and screening process to ensure the parts meet the requirements set forth in established reliability specifications such as the MIL-SPECS.

Today, however, many new satellite communication (satcom) applications are

being launched into low-Earth orbit (LEO), which is the area of space from 120 to 1200 miles above the Earth (see **Figure 1**). These satellites, which are increasingly being designed by commercial “new space” companies, can be made much smaller than GEO satellites, but because of their proximity to the Earth, the coverage area is also much narrower. This means multi-satellite constellations are needed to provide continuous and reliable low latency coverage, making cost a much bigger consideration when designing LEO satellites versus GEO satellites. As a result, many “new space” companies have adopted the use of reliable COTS parts for LEO satellites, reducing the time and expense involved in the traditional rigorous space qualification and screening process.

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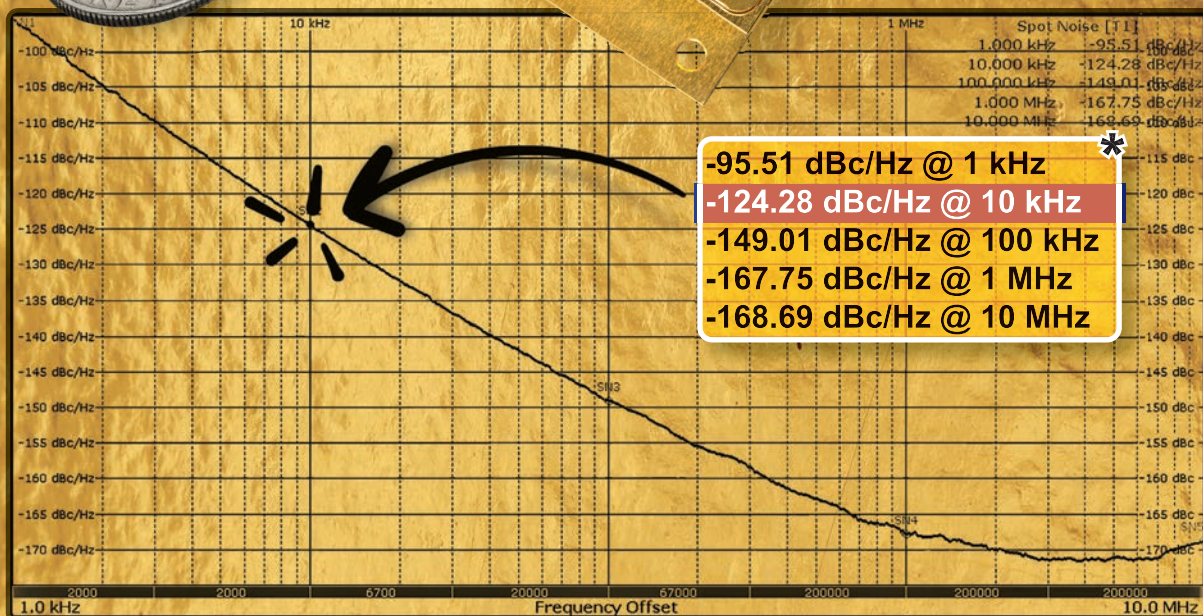
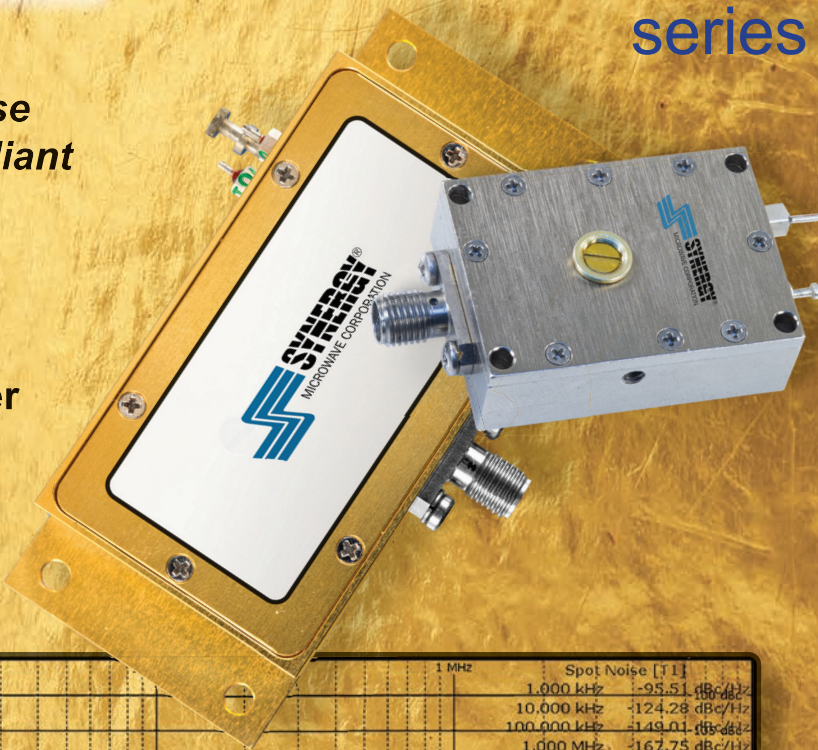
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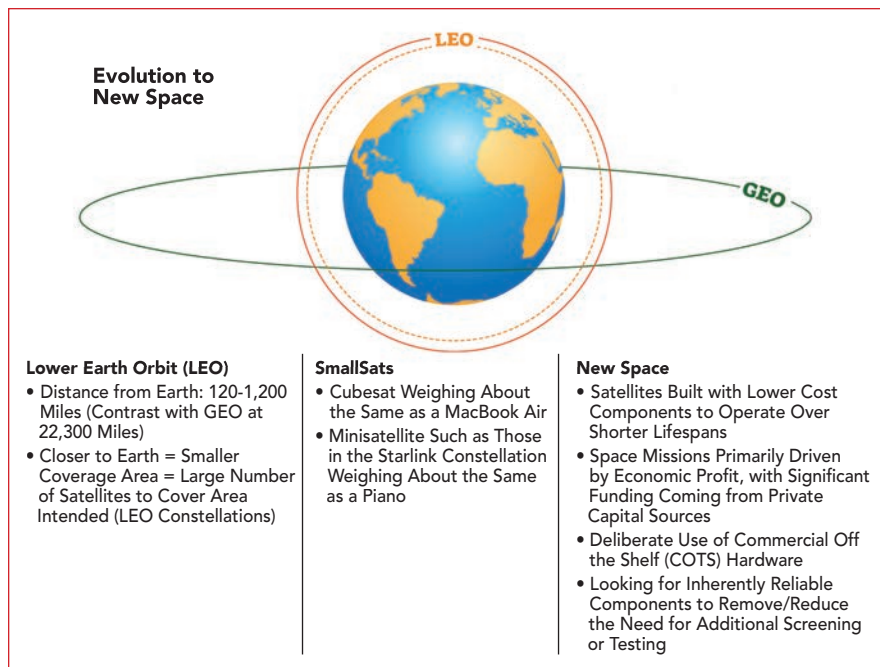


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▲ **Fig. 1** Reducing the cost of launching a satellite into orbit has enabled a new generation of innovation in space.

WHAT DOES NASA CONSIDER A COTS PART?

To start, it is important to understand how NASA has defined COTS parts. In a recent webinar, "Phasing in COTS Electrical, Electronic, and Electromechanical (EEE) parts in NASA,"² NASA Chief Safety and Mission Assurance Engineer Jesse Leitner described COTS parts as "parts where the manufacturer solely establishes and controls the specifications for performance, configuration and reliability." This includes defining the design, materials, processes and testing used, without considering additional requirements by users or external organizations. COTS parts are typically sold through commercial distributors.

Historically, many organizations have associated COTS parts with low reliability. But through this NESC study, NASA determined that high volume parts built by a supplier you know and trust are likely to be extremely reliable. Simply put, suppliers want to build parts that their customers will continue to buy. Providing high volumes of unreliable parts is not the way to do that. COTS does not mean the part is not qualified, not screened or not tested. Instead, the qualification, screening and testing is just not defined by the government or other external

party. In short, the study showed that COTS parts can provide reliability for space applications if the parts are produced at high volumes and are from reputable vendors that perform 100 percent vendor electrical testing and screening, covering all datasheet parameters and not testing beyond intended usage.

GAPS IN TRADITIONAL SCREENING METHODS

For many decades, NASA felt that using MIL-SPECs was the only reasonable approach aerospace engineers could take to guarantee reliability when procuring parts for mission-critical and costly space applications. These standards originated in the U.S. Department of Defense because of the need for uniformity and interchangeability of parts across the world. As a result, these quality specifications cover the most extreme range of conditions, and the U.S. government controls the drawings, requirements and specifications. Therefore, purchasing components that were tested using MIL-SPECs became the best way to try to guarantee reliability for parts used in space systems.

The NESC study has shown, however, that MIL-SPEC testing for some parts may arbitrarily link that part with reliability. This is because MIL-SPEC

testing is done using generic specifications that may not represent actual usage or manufacture. Parts may be over tested using standard MIL-SPEC screening practices, which can even negatively impact reliability.

NASA Screened COTS Parts

NASA screened COTS parts are parts that are screened outside of the MIL-SPEC "catalog" of parameters. These parts may be screened and/or qualified using guidelines such as NASA specification EEE-INST-002.³ The purpose of this specification is to establish baseline criteria for selection, screening, qualification and derating of EEE parts. It defines three levels of screening:

- Level 1: The highest reliability standard for missions of five years or longer
- Level 2: A high reliability standard for missions of one to five years
- Level 3: Standard reliability, standard lot acceptance inspection for missions of 12 to 18 months.

When using this approach, while not required, various MIL-SPEC tests are typically performed on parts to test for reliability. Again, since this type of testing is not based on the part's datasheet, it may lead to over testing relative to the application of the part. The NESC study showed that this option may yield the greatest uncertainty for reliability, especially if the COTS part being tested is a low volume part.

Testing COTS Parts Using Traditional Reliability Standards

In the NESC study, NASA made it clear that manufacturers of COTS parts can perform testing using established standards as they see fit, and the part will still be considered a COTS part if that testing and screening is the choice of the manufacturer. For example, the manufacturer may choose to test parts to demonstrate reliability using the well-known AEC-Q200 Stress Test Qualification for Passive Components standard, or a manufacturer may choose to include MIL-SPEC tests as part of the part number. From NASA's perspective, if the manufacturer chooses to perform these tests and provide the data, it counts as a COTS part.

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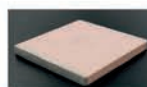
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WHEN AND HOW TO USE COTS PARTS

Phase 1 of the NESC report also provides guidance on deciding when and how to use COTS parts. First, the report shows how NASA

has traditionally defined how to make this decision based on mission and instrumentation risk (see **Table 1**). The NESC study then maps this traditional risk class chart to mission types and part grades that one

would find in the EEE-INST-002 standard (see **Table 2**). Defined this way, Class D missions, which include systems such as CubeSats (a type of SmallSat) or the experimental payloads on the International Space Station, are good candidates for including COTS parts.

In addition to understanding the risk classification of a system, the NESC study recommends selecting parts based on the project's mission, environment, application and lifetime (MEAL) requirements. More specifically, this means considering the following for each aspect:

- Mission – Risk classification, risk posture, schedule, cost and parts requirements
- Environment – Radiation, thermal, vacuum, etc.
- Application – Fault tolerance, architecture, size, weight and power, performance, etc.
- Lifetime – Mission lifespan and system operating conditions during the mission.

NASA'S RECOMMENDATIONS FOR USING COTS PARTS

Overall, in Phase 1 of the NESC study report, NASA conveys there are many suitable applications, such as LEO satcom devices, that could benefit from the reduced costs of using COTS parts.

To successfully determine the COTS parts that will meet a system's MEAL requirements, NASA recommends establishing a good relationship with an industry-leading parts manufacturer (ILPM). An ILPM is defined by NASA as a COTS parts manufacturer that produces high-quality and reliable parts that do not require additional screening and lot conformance testing. It is important to note there is no official list of ILPMs, and each organization using COTS parts needs to define acceptable ILPMs.

When possible, NASA recommends establishing a relationship with a company that has flight heritage. Additionally, talk with potential suppliers to ensure they respect the part's datasheet and do not screen parts outside datasheet levels, as this can actually reduce reliability.

USE COTS PARTS ALREADY TESTED FOR RELIABILITY

COTS parts can include con-

TABLE 1

MISSION AND INSTRUMENT RISK CLASSIFICATION CONSIDERATIONS

Priority (Relevance to Agency Strategic Plan, National Significance, Significance to the Agency and Strategic Partners)	Very High	Class A
	High	Class B
	Medium	Class C
	Low	Class D
Primary Mission Lifetime	Long, > 5 years	Class A
	Medium, 3 to 5 years	Class B
	Short, 1 to 3 years	Class C
	Brief, < 1 year	Class D
Complexity and Challenges (Interfaces, International Partnerships, Uniqueness of Instruments, Mission Profile, Technologies, Ability to Re-service, Sensitivity to Process Variations)	Very High	Class A
	High	Class B
	Medium	Class C
	Low	Class D
Life-Cycle Cost	High	Class A
	Medium to High	Class B
	Medium	Class C
	Medium to Low	Class D

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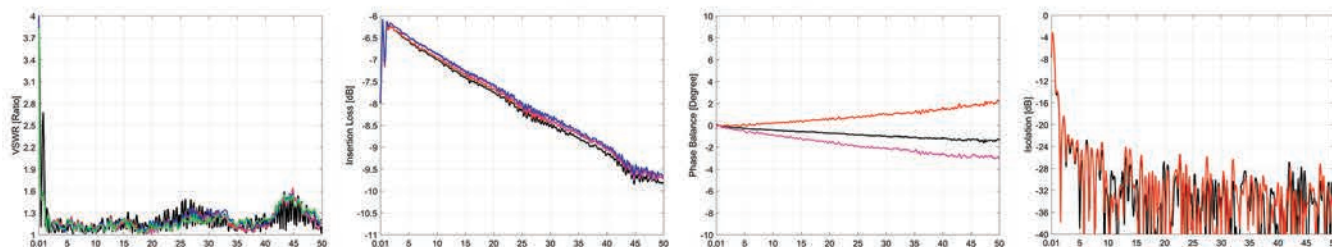
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SA-06-912	4	DC~2	1.7 (Typ.)	1.7 (Typ.)	1.5 (Typ.)	±0.2 (Typ.)	±2 (Typ.)	12 (Typ.)
		2~26.5	1.6	1.6	2.8	±0.4	±4	18
		26.5~50	1.7	1.7	4.0	±0.4	±5	20

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TABLE 2

JPL CLASSIFICATION FROM PHASE 1 OF THE NESC STUDY

Project Category	1	2		3
Mission Class	Class A	Class B	Class C	Class D
Mission Type	Human Space Flight	Non-Human Space Flight or Science/Robotic	Small Science (Human or No-Human)	Smaller Science (Human or Non-Human)
Part Grade	Grade 1	Grade 2	Grade 3	COTS
Qualification Level	Space	Full Military	Low Military	Commercial

sumer, industrial, commercial hi-rel, manufacturer hi-rel and industry hi-rel parts. As noted, when testing, manufacturers have the option to define hi-rel parts using established methods, such as those defined in AEC-Q200 or MIL-SPECS. However, as an end user of COTS parts, it is important to be aware that, depending on the MEAL requirements of an application, an AEC-Q200-qualified part may not cover all the reliability requirements for the mission. Instead of solely looking for parts that are AEC-Q200-qualified or tested to certain MIL-SPECS, it is best to work with an ILPM to under-

stand where potential gaps may exist between the MEAL requirements and the AEC-Q200 qualifications or MIL-SPEC testing.

For example, in 2018, The Aerospace Corporation presented a discussion on the differences between AEC-Q200 parts and MIL-SPEC parts in its "Guide to Using Automotive-Grade EEE Parts in Space Applications."⁴ The report shows a comparison between MIL-PRF-123 and AEC-Q200 for capacitors and highlights the following tests that should be discussed with the manufacturer: radiographic inspection, thermal shock, voltage condition-

ing, terminal strength and life test. In general, this is a good example of the types of test topics that should be discussed with an ILPM during parts selection.

WHAT IS NEXT FOR COTS PARTS IN SPACE?

Even with the recommendations provided in Part 1 of the NESC study, there is not a one-size-fits-all approach to selecting COTS parts for space applications. A good start to determining what could work best for an application is to understand some of the more traditional qualification and screening requirements, such as those defined in the white paper "Ready for Launch: Understanding the Nuances of Space-Level Qualification and Screening of Filters."⁵ Then, develop relationships with ILPMs to work together, discuss the project's MEAL requirements and determine how to effectively select proven and reliable COTS parts for the space application.

NASA will release Phase 2 of the NESC study later this year, providing information to dispell myths about using COTS parts and NASA's recommendations for new approaches for reliably using COTS parts from ILPMs. ■

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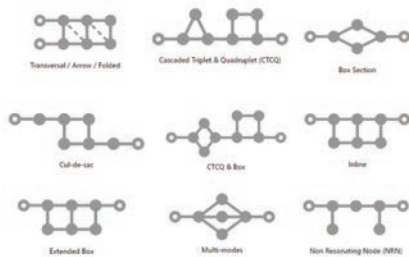
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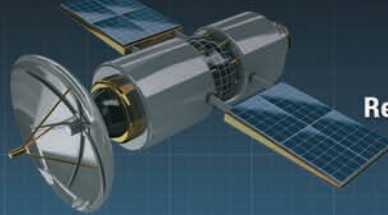
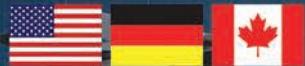
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Increasing restrictions are one of the biggest challenges related to the growth of 5G applications, particularly shrinking the size and form factor of the components. Design engineers focused on filter designs must spend much time and effort to determine a resonator layout that will meet these dimensional requirements; the restrictions add risk to the design workflow, such as reducing the out-of-band rejection or power handling. To meet the size and weight requirements without sacrificing RF performance, designers must have greater design flexibility to consider alternative topologies. The challenge, however, is few software tools are available to help designers explore topologies and options that will meet the design goals.

SynMatrix is one of the most advanced RF filter design and test tuning platforms, which reflects the company's mission to significantly reduce the time to engineer and manufacture complex RF filters. Pursuing this goal, SynMatrix has released several innovative functions during the past two years to accelerate the design workflow. Recently, SynMatrix released an upgrade for creating topology designs. Previously, users had the freedom to create and edit their own topologies by clicking on an easy-to-use graphical interface; however, this required having a thorough knowledge of filter design and topologies. To help less experienced designers, SynMatrix has introduced a library with thousands of practical topologies that can be selected to best

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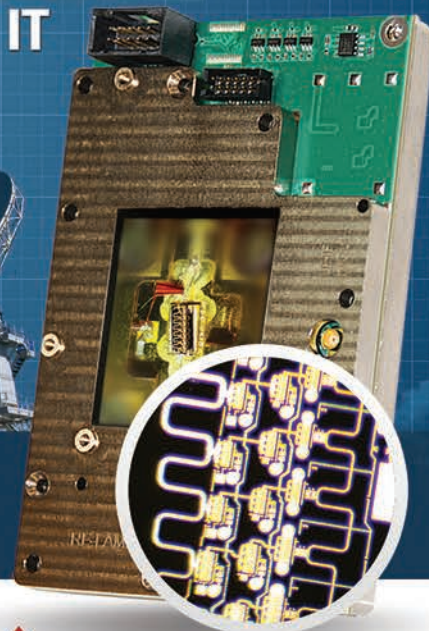
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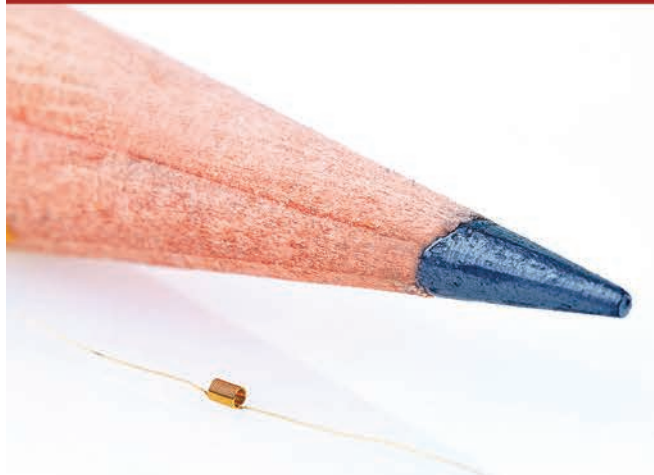


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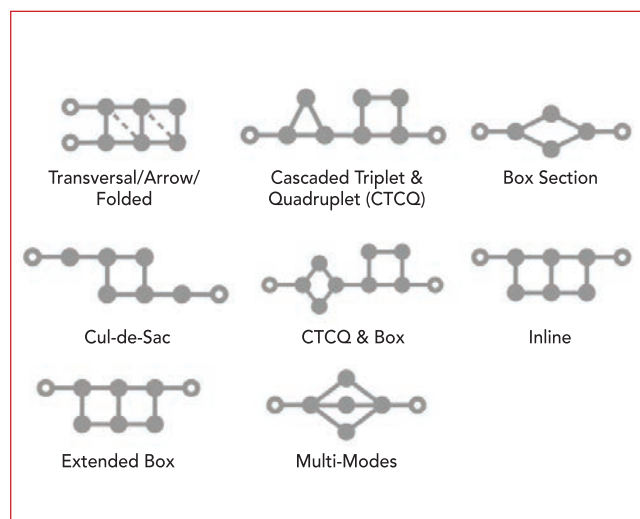


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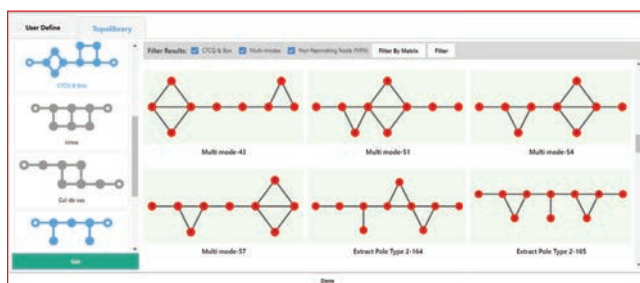
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▲ Fig. 1 SynMatrix topology library.



▲ Fig. 2 Graphical interface for generating the coupling matrix.

fit the application.

This new integrated topology library (see **Figure 1**) includes several categories and types, including transversal, arrow, box section, inline, cul-de-sac, non-resonating node, extended box and multi-modes. SynMatrix's topology library considers the more practical applications users may face, offering hybrid modes that mix different topology types.

The design workflow begins with specifications, where designers input the filter order and transmission zero information. Then, users select from a large library of topologies and generate the corresponding coupling matrix. The coupling matrix can be generated from a standard topology list and, using an advanced coupling matrix reduction technique (see **Figure 2**), generate the coupling matrix from a mixed topology matrix. Examples of these mixed topology structures include the cascaded triplet (CT) or cascaded quadruplet (CQ) mixed with box section; non-resonating node mixed with CT or CQ; and multi-mode mixed with CT or CQ.

SynMatrix has implemented a thorough and comprehensive method to explore all possible combinations from these mixed topologies, generating thousands of possibilities from the different combinations. To maintain an easy-to-use experience without overwhelming users, SynMatrix offers a filter function within the graphical interface that helps users choose the desired topology by selecting a fixed coupling path



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At IMS2023 we will have several focus themes to highlight a number of areas of RF and microwave engineering that are of topical interest or impact. These themes are:

- **Systems & Applications**
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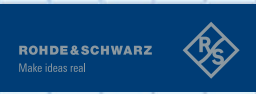
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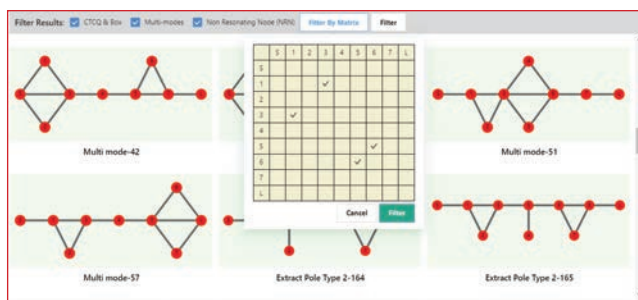




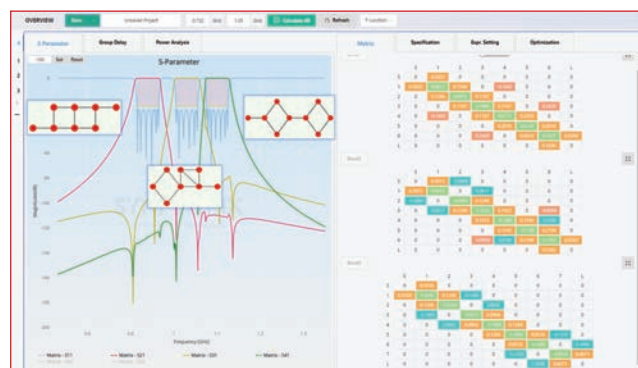
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ProductFeature



▲ Fig. 3 Interface for selecting the coupling path.



▲ Fig. 4 Completed filter simulation.

(see **Figure 3**). This feature augments the current interface, so users opting to construct their own coupling and topology structures can still use the prior “check mark” table interface. This gives designers the full range of options, which they choose to best support their backgrounds or the application.

Using the same workflow and user experience, the new topology library supports several filter types, including multiband, diplexer and triplexer (see **Figure 4**). Considering data analysis and diagnostics, SynMatrix’s Computer-Aided Tuning (CAT) platform now supports more applications. Designers can use CAT to evaluate these newly supported topologies, such as box section and its mixed format, cul-de-sac, arrow and transversal.

The introduction of the SynMatrix topology library expands the flexibility for filter designers, with more capability to address the challenging design requirements driven by 5G. It increases design engineering capabilities, saves time in the development and helps identify and avoid downstream RF performance problems that may not be apparent at the start of the design workflow. By using a comprehensive set of tools and topologies, SynMatrix quickly unblocks many of the challenges facing design engineers, simplifying the design process and yielding more successful designs.

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www.synmatrixtech.com

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AnaPico Switzerland has improved the performance of its 22 GHz frequency synthesizer, launched earlier this year, extending the frequency range to 44 GHz and significantly reducing the single sideband (SSB) phase noise. Most of the other functions of the new APMSYN40 wideband synthesizer remain the same as in the earlier model.

The frequency range of the APMSYN40 is 10 MHz to 44 GHz, and it has a switching time of about 10 μ s and an output power range from 0 to 23 dBm. The SSB phase noise at a 20 kHz offset from a 1 GHz carrier is -145 dBc/Hz, with a 10 GHz carrier, it's -120 dBc/Hz. Resolution is 1 mHz for frequency and 0.5 dB

44 GHz Low Phase Noise Synthesizer Supports Phase-Coherent Channels

for power. The frequency accuracy is calibrated to ± 30 ppb and temperature stability is ± 100 ppb over the operating temperature range from 0°C to 50°C.

The synthesizer is available in a well shielded, passively cooled, compact flange-mountable module of 150 x 60 x 30 mm³, weighing under 0.5 kg and consuming less than 20 W power. It has an Ethernet communication port for connecting to a PC and is controlled with either a graphical software interface or SCPI commands.

The APMSYN40 supports external references of 100 MHz and 1 GHz. Multiple units can be connected for multi-channel, phase-coherent sources, generating the main 1 GHz refer-

ence frequency in one unit and looping it to the others. Phase-coherence is approximately ± 0.5 degrees over 10 hours with all channels at 5 GHz.

This wideband, fast switching synthesizer is well-suited for applications requiring a controlled phase difference between multiple channels—radar, electronic warfare, beamforming, quantum computing—or a single unit can be used as a system clock.

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Compact, 10 MHz to 22 GHz Preamplifier Improves EMC Testing

A new RF preamplifier from Langer EMV-Technik was developed to boost the weak signals encountered with electromagnetic compatibility (EMC) measurements. In addition to the low signal levels, EMC measurements are often challenging because of insufficient sensitivity of the measuring instruments.

To address this, Langer EMV-Technik's PA 2522 preamplifier provides 25 dB gain across the frequency range from 10 MHz to 22 GHz, enabling harmonics to be measured to 22 GHz. The preamplifier has 3 dB noise figure across most of the frequency range, gradually increasing at the band edges.

The PA 2522 was designed to be used with Langer EMV's matching near-field probe connected at the input. The output of the preamplifier connects to the 50 Ω input of a spectrum analyzer or oscilloscope, boosting signals while protecting the measuring analyzer or scope from overload. The preamplifier's 1 dB compression point is 14 dBm at 10 GHz.

The PA 2522 is assembled in a compact housing, 38 x 50 x 14 mm³, with an SMA female input and SMA male output connectors. A separate adapter supplied with the PA 2522 converts AC to the 7 to 12 V DC required to power the unit, which draws 190 mA. The small size of the

preamplifier makes it versatile and easy to integrate into an EMC testing environment.

Langer EMV-Technik focuses on EMC, offering interference emission and immunity measurement technology, test systems, training and consulting to support IC and module development. The company's goal is using its capabilities to help designers improve strategies for mitigating EMC issues during development. Langer EMV-Technik's products are handcrafted in Germany.

Langer EMV-Technik GmbH
Bannewitz, Germany
www.langer-emv.com



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Analog Devices

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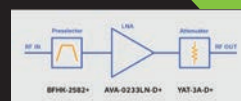


Every Block Covered: Noise and SNR in a Simple Microwave Front-End

The purpose of this short applications note is to square-up noise, noise floor, bandwidth and signal-to-noise ratio (SNR) in general, and to compute these parameters for a basic, three-component RF front-end.

Mini-Circuits

<https://blog.minicircuits.com/noise-and-signal-to-noise-ratio-snr-in-a-simple-microwave-front-end/>



Panasonic's Online Simulator

Panasonic's online simulator can calculate impedance matching, wavelength and transmission loss for each frequency band in electrical lines like MSL and stripline.

Panasonic

<https://util01.industrial.panasonic.com/www/utilities/em/msl-sim/>

Fully Automatic Production System

Check out a video demonstration of RF-Lambda's fully automatic production system.

RF-Lambda

<https://bit.ly/3QTQE7e>



Online impedance simulator



This simulator intends to assist you in designing with Panasonic Materials. Approximate value of IMPEDANCE, WAVELENGTH and TRANSMISSION LOSS for your PCB can be simulated.

Meet Harrison Osbourn – Signal Hound's New Owner and CEO

Learn more about Signal Hound's new owner and CEO, Harrison Osbourn, by reading the recent interview conducted by The Portland Business Journal. Full article linked below.

Signal Hound

<https://signalhound.com/news/harrison-osbourn-interview/>



Waterproof (IP68 Rated) RF Cable Assemblies



SV Microwave offers a wide range of IP67 and IP68 waterproof cable assemblies designed to withstand rigorous environments and harsh elements. SV's line of waterproof cable assemblies include o-ring sealed connectors to 1 x 10⁻⁸ cc/sec, making them ideal for high pressure, harsh environment applications and for the prevention of dust, liquid or gas leakage.

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COMPONENTS

Taps and Splitters



The DOCSIS 3.1/4.0 standards offer sufficient data rate potential, provided a high-quality coax network is in place. The trick with modern passive components

is to push the physical limits as far as possible like the latest developments from AXING do. All components meet the highest demands in terms of surge immunity, shielding, intermodulation resistance and port-to-port decoupling, in addition to the "traditional" RF characteristics such as low through-loss and very good matching/return loss.

AXING AG
www.axing.com

SPST Absorptive Switch



Model SKS-2242946035-0303-A1-M is an absorptive SPST switch that controls signals from 220 to 290 GHz. Insertion loss is 6 dB with typical isolation

of 35 dB. The RF ports are WR-03 waveguide with UG-387/U-M anti-cocking flanges. The switch accepts a TTL-level control signal and achieves a switching speed of 100 ns. The maximum RF power is +5 dBm. The switch requires positive and negative bias voltages of +1 and -2 V. Dimensions are $1.0 \times 1.0 \times 0.75$ in.

Eravant
www.eravant.com

Waveguide Isolators



HASCO introduces a new line of waveguide isolators. These waveguide isolators operate from 26.5 to

140 GHz. The insertion loss in the forward direction is minimized to allow for the full available power from the signal source-isolator combination. Applications are test labs, sub-assemblies, automotive industry and mmWave test systems.

HASCO
www.hasco-inc.com

Voltage-Variable Attenuator



Mini-Circuits' model PVA-453-34+ GaAs MMIC voltage-variable attenuator (VVA)

features a pair of attenuators supplied in a surface-mount technology (SMT) package measuring 3.5×2.5 mm with frequency range of 10 to 45 GHz. Attenuation is set by independent control voltages from -4 to 0 VDC. The RoHS-compliant VVA boasts typical attenuation ranges of 39.5 dB to 20 GHz, 40.0 dB to 40 GHz and 33.9 dB to 45 GHz and can handle as much as +23 dBm RF input power.

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connectors with 086 semi-rigid cable (outer diameter 2.2 mm). It can be bent to any requested shape with reliable and excellent mechanical and electrical performance, the shielding effectiveness of the assembly is less than -120 dB, and the maximum VSWR of the assembly is 1.30:1 at 40 GHz and 1.40:1 at 50 GHz, as well as the maximum cable loss is 5.27 dB/m at 40 GHz and 6.1 dB/m at 50 GHz, respectively. It is well-suited for the internal and external connection of microwave equipment, test instruments and fixtures.

Fujian Micable Electronic Technology Group Co., Ltd.
www.micable.cn

DuraWave™ PS43 Test Port Cables



Swift Bridge Technologies' DuraWave™ PS43 test port cables were developed to exceed OEM's cable performance through 43.5 GHz. Insertion

losses, return losses, phase stability and insertion loss stability with flexure are guaranteed not to exceed certain limits. Insertion losses at 43.5 GHz are typically 30 to 40 percent lower than the OEM's test port cables with VSWR < 1.25 (< -18 dB S_{11} and S_{22}). DuraWave™ PS43 is available with precision 2.92 and 2.4 mm connectors to interface with your particular analyzer model.

Swift Bridge Technologies
www.swiftbridgetechnologies.com

AMPLIFIERS

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Exodus Advanced Communications' 18.0 to 26.5 GHz, 200 W solid-state amplifiers are another industry first from Exodus. Designed for

high field level EMC testing, Mil-Std 461(RS103) standards as well as other high-power applications. Exodus Model AMP4065B-LC is a 12U design providing outstanding power/gain flatness, forward/reflected power monitoring in both dBm and W, VSWR, voltage/current and temperature sensing for superb reliability and ruggedness. Unprecedented reliability compared to TWTs, 53 dB gain including gain control and -20 dBc harmonics. 10, 20, 40, 60 and 100 W versions available.

Exodus Advanced Communications
www.exoduscomm.com

SGA/SGN Series SSPAs



KRATOS General Microwave's SGA/SGN Series SSPAs offer GaAs/GaN technology reliability

that can be customized to meet specific pulse or CW output powers. The product line supports both X-Band and Ku-Band applications with bandwidths up to 10 percent and offers peak power outputs up to 400 W. Designed for demanding defense, aerospace and satellite communication applications. General Microwave SSPAs have excellent power efficiency with demonstrated field proven performance and

NewProducts

reliability. General Microwave's vertical integration process affords flexible layouts and architectures to meet individual specifications for electrical, mechanical and environmental parameters.

KRATOS General Microwave
www.kratosmed.com

2.0 to 8.0 GHz Amplifier

VENDORVIEW



Quantic PMI Model Number PMI-AFD4-020080-23P-SMA is a 2.0 to 8.0 GHz

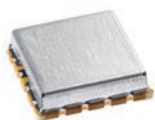
amplifier that has a maximum gain of 35 dB, maximum gain flatness of ± 2.0 dB, a maximum noise figure of 3.5 dB and a maximum VSWR of 2.0:1. This model is outfitted with SMA female connectors in a housing that measures $1.83 \times 0.76 \times 0.20$ in.

Quantic PMI
www.pmi-rf.com

SOURCES

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The Z-COMM CRO6835X3-LF provides a clean signal source at 6835 MHz for satcom, radar and atomic clock applications to name a few. Phase noise is -105 dBc/



Hz at 10 KHz and -127 dBc/Hz at 100 KHz. The unit provides a tuning range of 6810 to 6860 MHz within 0.5

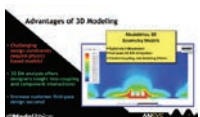
-8 Vdc, with harmonic suppression of -25 dBc typical. Current consumption is just 24 mA from a 5 Vcc supply. Industry standard 0.5×0.5 in. SMT package, available on tape and reel, supports automated production lines.

Z-Communications Inc.
www.zcomm.com

SOFTWARE

COMPLETE+3D Library

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Modelithics announced the release of version 22.4 of the COMPLETE+3D Library for use with Ansys HFSS. Included

in this library are over 370 highly scalable Microwave Global Models™ for capacitor, inductor and resistor families from many popular vendors. Also included is Modelithics' collection of over 500 3D electromagnetic (EM) geometry models for inductors, capacitors, filters, packages and connectors. With both circuit and 3D EM models, the Modelithics COMPLETE+3D Library now includes over 30 vendors for more than 850 models representing over 25,000 individual components.

Modelithics Inc.
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Aaronia AG
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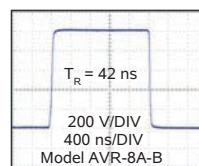


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Avtech Electrosystems Ltd.
http://www.avtechpulse.com/





Review by: Benoit Derat,
Rohde & Schwarz GmbH & Co. KG



Bookend

RF Circuits and Applications for Practicing Engineers Mouqun Dong

RF Circuits and Applications for Practicing Engineers is the book every RF PCB-based circuit and system engineer starting in the wireless industry has ever dreamed of. Take 25 years of premium experience in RF design from Mouqun Dong and put them in a bit less than 400 pages, here is what you get: a very practical manual which bridges gaps between traditional education and daily work of the RF engineer. Which RF designer has never struggled in understanding component datasheets and trying to devise which specifications might be more critical than others for a given application? From his strong theoretical and professional background, Dr. Dong helps with that, by clarifying the variations in industry terms and definitions of key parameters like the noise figure and which to use for certain purposes. The book is structured to brush a wide

variety of topics with only the necessary mathematics to understand the main principles and how to put them in practice. Starting from the theory of noise and S-parameters and their applications in circuit design, Dr. Dong then proposes three chapters on RF amplifier designs and operating principles of power amplifiers. A particularly interesting part is the discussion on stability analysis of amplifier circuits, relevantly demonstrating that trying to achieve unconditional stability across frequency at all cost and under all circumstances is an actual misconception. The next chapters cover a panel of subjects from base principles of RF transceiver system designs in wireless communications, to passive components used in RF circuits (lumped elements and their parasitic effects, directional couplers, hybrids, etc.), solid-state switches and a short section on RF measurements (S-parameters, spectrum analysis, phase noise and error vector magnitude, noise figure, power and non-linearities). This book

is far from addressing all RF problems that the practitioner will encounter in a career and does not pretend to do so. It gives, however, a fantastic insight into the mind of someone who has long exercised the discipline of PCB-based RF system designs and is willing to share his experience. It is a very valuable resource for starting RF engineers willing to learn or experienced ones needing to brush up on the theory behind the practice.

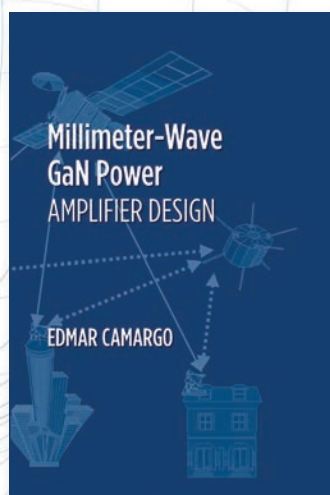
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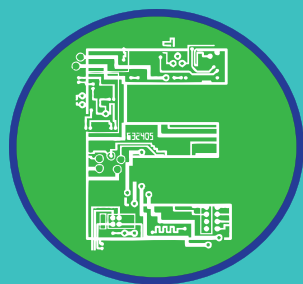


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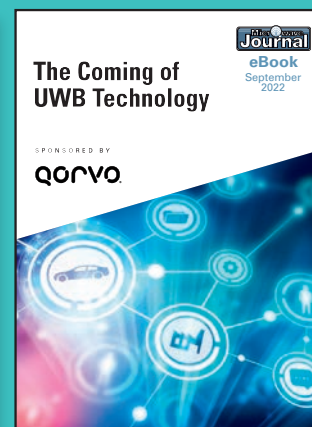
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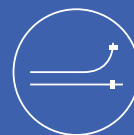
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ERZIA: Staying Ahead to Go Further



ERZIA had an inauspicious start, prompted by the telecom collapse in 2001. Luis García, who was working at Ericsson in Sweden, returned to Spain and began consulting with the European Space Agency, which was the genesis of ERZIA in 2002. García's design consulting led to the company's first hardware in 2005, built for the LISA Pathfinder, a space project to test a laser interferometer space antenna for a gravitational wave observatory. While the space market sustained the early years and established the company's bona fides, the "lumpiness" of space programs wouldn't support continuous growth, so García expanded his focus to defense—now 80 percent of ERZIA's business—and building a portfolio of standard components.

New products are initiated either as custom designs for programs or when multiple customers request a similar product. After development, generic products are added to the catalog. Since the first products released in 2011, the catalog has grown to power and low noise amplifiers, suspended substrate filters, RF drivers for acousto-optic tunable filters and modulators and converters for civil and military satellite communications. ERZIA also supplies complex assemblies to system and platform integrators, from multi-function modules to line-replaceable units.

The products in the catalog reflect the challenging design goals ERZIA has achieved. Examples: In 2019, it released a 300 W pulsed power amplifier covering 8.5 to 9.8 GHz for radar applications. The design uses GaN transistors to maximize output power and power-added efficiency, typically 23 percent. For satellite links, ERZIA developed a low noise amplifier covering 17.7 to 22 GHz with 1.2 dB typical noise figure, calling it the best Ka-Band LNA for airborne systems. Suspended substrate filters are the latest products to be developed,

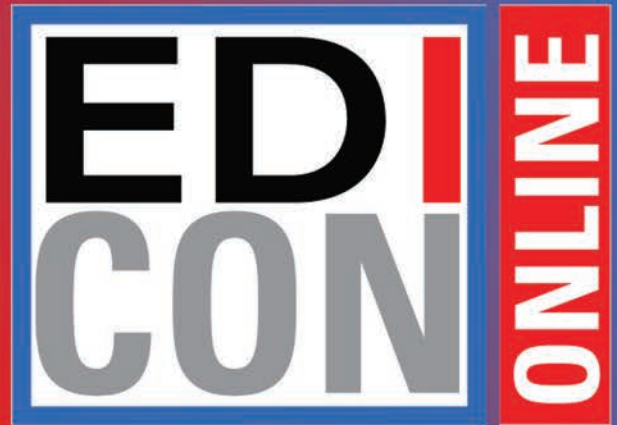
introduced in 2021. This filter technology provides highly selective band edges with the advantage of a small footprint. Suspended substrate designs can be combined with microstrip or lumped elements to achieve more complex filter responses.

ERZIA is based in Santander, a port city on the northern coast of Spain. It occupies two buildings, in one a 900 m² facility for chip-and-wire assembly comprising epoxy die attach, wire bonding with pull testing and epoxy sealing. For high power assemblies, ERZIA has perfected its epoxy process to attach GaN devices to high thermal conductivity materials such as CuMo. Completing ERZIA's internal manufacturing capabilities are CNC machines for metal fabrication and environmental and full electrical testing up to 100 GHz. ERZIA doesn't build its own semiconductors, enabling it to select the best suppliers for an application. Its quality guidelines are based on the European Cooperation for Space Standardization (ECSS), EN9100 and the UNE-EN ISO 9001:2015 standards for design and manufacturing.

ERZIA's singular capabilities, space heritage with the utmost quality, relationship with the local University of Cantabria and European location have fostered its capabilities and growth. In Europe, ERZIA is considered a local supplier, increasingly important to the EU as countries secure supply chains to guard national security. Beyond its technology and location, ERZIA has developed an enviable reputation for flexibility and responsiveness, which draws customers from Israel, North America and Japan. This flexibility and responsiveness reflect the culture and philosophy of ERZIA's small team of some 40 professionals, who are passionate about solving technical challenges, the systems their products enable and quality. As they say, it's this commitment to staying ahead that enables their customers to go further.

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C8731	Dual	0.009-250	1000	40	0.40	N-Female	10.5 x 3.0 x 2.0
C11462	Dual	0.009-400	500	40	0.45	N-Female	6.7 x 2.28 x 1.69
C8510	Dual	0.009-1000	500	40	0.45	N-Female	6.7 x 2.28 x 1.69
C5047	Dual	0.01-100	4,000	50	0.15	7/16-Female	10.0 x 4.16 x 3.5
C1979	Dual	0.01-100	10,000	60	0.10	LC-Female	2.0 x 6.0 x 4.5
C5086	Dual	0.01-250	250	40	0.50	N-Female	5.2 x 2.67 x 1.69
C5100	Dual	0.01-250	500	40	0.40	N-Female	10.5 x 3.0 x 2.0
C5960	Dual	0.01-250	1,000	50	0.40	N-Female	10.5 x 3.0 x 2.0
C1460	Dual	0.01-250	2,000	50	0.15	N-Female	10.0 x 3.0 x 2.0
C4080	Dual	0.01-250	3,500	50	0.20	N-Female	10.0 x 4.6 x 3.5
C11026	Dual	0.01-220	5,000	60	0.10	LC-Female	12.0 x 6.0 x 4.5
C8390	Dual	0.01-250	10,000	60	0.10	LC-Female	12.0 x 6.0 x 4.5
C5339	Dual	0.01-400	200	40	0.50	N-Female	5.2 x 2.67 x 1.69
C6047	Dual	0.01-400	500	40	0.50	N-Female	5.2 x 2.67 x 1.69
C2630	Dual	0.01-1000	100	40	0.60	N-Female	5.0 x 2.0 x 1.51
C6021	Dual	0.01-1000	500	40	0.45	N-Female	6.7 x 2.28 x 1.69
C6277	Dual	0.01-1000	500	50	0.45	N-Female	6.7 x 2.28 x 1.69
C11146	Dual	0.01-1000	500	43	0.45	SC-Female	6.7 x 2.63 x 2.20
C11047	Dual	0.01-1000	1,000	43	0.45	SC-Female	6.7 x 2.63 x 2.20
C11161	Dual	0.01-1000	1,000	50	0.45	SC-Female	6.7 x 2.63 x 2.20
C1795	Dual	0.1-1000	100	40	0.50	N-Female	5.0 x 2.0 x 1.51
C5725	Dual	0.1-1000	500	40	0.50	N-Female	5.2 x 2.28 x 1.69
C11077	Dual	0.1-1000	1,000	43	0.45	SC-Female	6.7 x 2.28 x 1.69
C3910	Dual	80-1000	200	40	0.20	N-Female	3.0 x 3.0 x 1.09
C5982	Dual	80-1000	500	40	0.20	N-Female	3.0 x 3.0 x 1.09
C3908	Dual	80-1000	1,500	50	0.10	7/16-Female	3.0 x 3.0 x 1.59
C6796	Dual	80-1000	5,000	60	0.20	1 5/8" EIA	6.0" Line Section
C8060	Bi	200-6000	200	20	0.40	SMA-Female	1.8 x 1.0 x 0.56
C8000	Bi	600-6000	100	30	1.10	SMA-Female	4.8 x 0.88 x 0.50
C10117	Dual	700-6000	250	40	0.20	N-Female	2.0 x 2.0 x 1.06
C10364	Dual	700-6000	500	50	0.20	7/16-Female	2.15 x 2.0 x 1.36
C10996	Dual	700-6000	700	50	0.20	7/16-Female	2.15 x 2.0 x 1.36
C11555	Dual	700-6000	1,000	50	0.20	7/16-Female	2.15 x 2.0 x 1.36
C10695	Dual	700-6500	500	50	0.20	7/16-Female	2.15 x 2.0 x 1.36